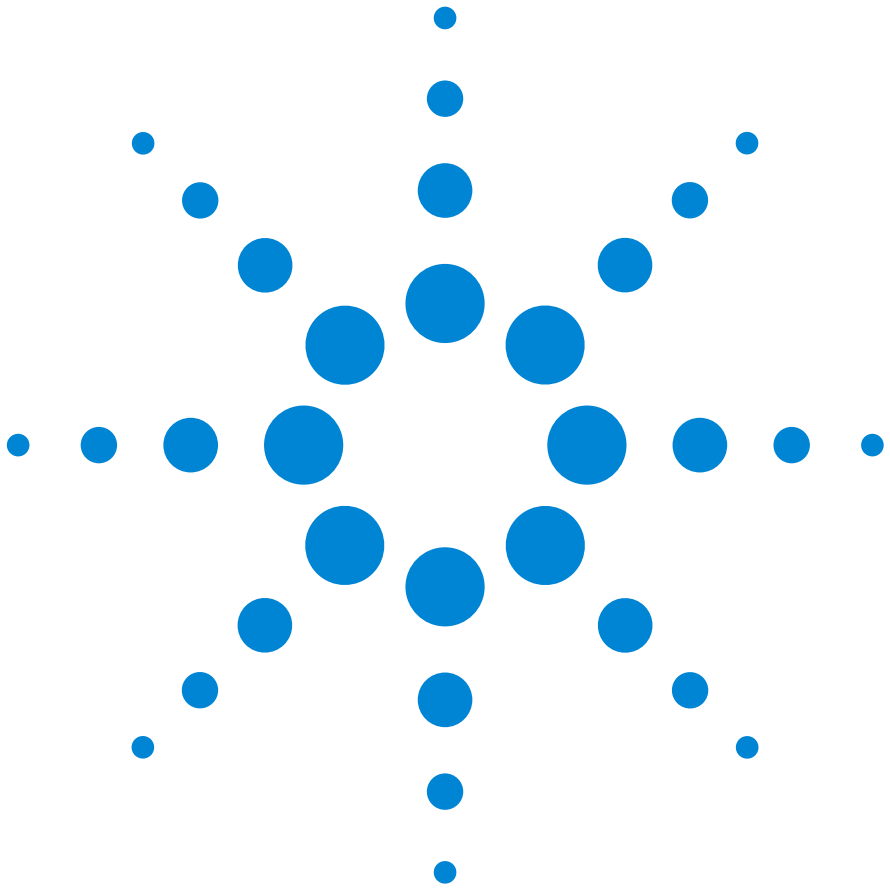

Agilent 10897B High Resolution VMEbus Laser Axis Board

Operating and Service Manual

Agilent Technologies

Operating and Service Manual

SERIAL PREFIX NUMBER: 3332

This manual applies to Agilent 10897B High Resolution VMEbus Laser Axis Board with the 3332.

SERIAL PREFIX NUMBERS NOT LISTED

For Serial Prefixes higher than those listed above, a "Manual Changes Sheet" is included with this manual. For Serial Prefixes lower than those listed above, refer to Section 8, "Manual Changes."

Agilent 10897B High Resolution VMEbus Laser Axis Board

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Printed: August 2000

Printed in USA

Manual part number 10897-90010

Certification and Warranty

Certification

Agilent Technologies certifies that this product met its published specification at the time of shipment from the factory. Agilent further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology (formerly National Bureau of Standards), to the extent allowed by the Institute's calibration facility, and to the calibration facilities of other International Standards Organization members.

Warranty

Agilent warrants Agilent hardware, accessories and supplies against defects in materials and workmanship for a period of 3 years from date of shipment. If Agilent receives notice of such defects during the warranty period, Agilent will, at its option, either repair or replace products which prove to be defective. Replacement products may be either new or like-new.

Agilent warrants that Agilent software will not fail to execute its programming instructions, for the period specified above, due to defects in material and workmanship when properly installed and used. If Agilent receives notice of such defects during the warranty period, Agilent will replace software media which does not execute its programming instructions due to such defects.

For detailed warranty information, see back matter.

Safety Considerations

General

This product and related documentation must be reviewed for familiarization with this safety markings and instructions before operation.

Before Cleaning

Disconnect the product from operating power before cleaning.

Warning Symbols That May Be Used In This Book

Instruction manual symbol; the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual.

Indicates hazardous voltages.

Indicates earth (ground) terminal.

or

Indicates terminal is connected to chassis when such connection is not apparent.

Indicates Alternating current.

Indicates Direct current.

Safety Considerations (contd)

WARNING

BODILY INJURY OR DEATH MAY RESULT FROM FAILURE TO HEED A WARNING. DO NOT PROCEED BEYOND A WARNING UNTIL THE INDICATED CONDITIONS ARE FULLY UNDERSTOOD AND MET.

CAUTION

Damage to equipment, or incorrect measurement data, may result from failure to heed a caution. Do not proceed beyond a *CAUTION* until the indicated conditions are fully understood and met.

Safety Earth Ground

An uninterruptible safety earth ground must be maintained from the mains power source to the product's ground circuitry.

WARNING

ANY INTERRUPTION OF THE PROTECTIVE GROUNDING CONDUCTOR (INSIDE OR OUTSIDE THE PRODUCT'S CIRCUITRY) OR DISCONNECTING THE PROTECTIVE EARTH TERMINAL WILL CAUSE A POTENTIAL SHOCK HAZARD THAT COULD RESULT IN PERSONAL INJURY. (GROUNDING ONE CONDUCTOR OF A TWO CONDUCTOR OUTLET IS NOT SUFFICIENT PROTECTION.) WHENEVER IT IS LIKELY THAT THE PROTECTION HAS BEEN IMPAIRED, THE PRODUCT MUST BE MADE INOPERATIVE AND BE SECURED AGAINST ANY UNINTENDED OPERATION.

For additional safety and acoustic noise information, see back matter.

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8.NC.NL.A.03.11.97.R1.J.CW4F

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Contents

Preface

Purpose

This manual provides general information, installation instructions, operating information, theory of operation, maintenance, exchange assembly details, manual change, and service information for the Agilent 10897B High Resolution Laser Axis Board.

Audience

This manual is intended for anyone who wants to: design the Agilent 10897B into an OEM system, supply additional capability to an existing compatible system, or needs the information in a lab environment for experimental puposes.

Prerequisities

A basic knowledge of computer operation with VMEbus, digital logic, laser measurement concepts, and the HP Laser Position Transducer System is required and assumed.

Reference Documentation

To use this manual, you should be familiar with the publications listed below:

- VMEbus Specification, Rev C.1 (IEEE P1014/D1.2),
- Agilent Laser and Optics User manual, part number 05517-90045,
- User-selected (system specific) VMEbus Control Processor manual.

1

General Information

Equipment Description

The Agilent 10897B High Resolution VMEbus Laser Axis Board is a register-based VME board. It converts reference and measurement signals from an Agilent laser head and measurement receiver to a 36-bit digital position word that is readable by a VMEbus system processor module over a VME backplane, and is available as a real time hardware output.

The Agilent 10897B board can also generate interrupts at any of the seven VMEbus interrupt levels (software programmable) for any of the following conditions: Reference or Measurement signal glitch or absence, interpolator loss-of-lock, or position counter overflow. The six position registers and the two velocity registers on the Agilent 10897B board may be read using 16- or 32-bit data transfers.

Compatibility

The Agilent 10897B board can replace the Agilent 10897A board in any application. The Agilent 10897B board will provide improved slew rate capability when it is combined with a laser head and receiver whose performance characteristics exceed those currently available (as of early 1995).

Type of Optics	Agilent 10897A	Agilent 10897B
Linear	800	1400
Plane Mirror	400	700
High Resolution	200	350

The Agilent 10897B board (as well as the Agilent 10895A board, Agilent 10896A board, Agilent 10896B board and the Agilent 10897A board) complies both electrically and mechanically with Rev C.1 of the VMEbus specification. However, the two outer rows of the P2 connector are not defined by C.1 and are commonly used for board-specific inputs and outputs. This is the case for the 10897B board (see Chapter 2). Inserting the 10897B board into a slot for another board may cause damage to either the 10897B board or the VMEbus backplane.

The Agilent 10896B Compensation Board is designed to work with the Agilent 10897B board and will not be damaged by inserting it into a VMEbus slot intended for the 10897B board. This allows P2 connector bussing common to all the Agilent 10897B boards in the system to continue to the P2 connector for the 10896B board. Do not plug an 10897B board into a slot intended for the 10895A board or vice-versa because the functions on the P2 connector are not all the same and damage may result.

Equipment Supplied

When Option 002 is ordered, the Agilent 10897B is supplied with a 2-Axis Interconnect Cable, Agilent Part Number 10895-60201. If Option 003 is ordered, a 3-Axis Interconnect Cable, Agilent Part Number 10895-60202 is supplied. (Options 004 through 007 are shipped in like manner.) Refer to Chapter 7 for option part numbers.

PC Board Identification

Agilent Technologies products have a two-section nine-digit plus one letter serial number attached to the product. The four-digit prefix (first four digits from the left) identifies a series of products manufactured identical to each other. The letter indicates the assembly plant location. The five-digit serial number is different for each product. If the serial prefix of your laser axis board(s) is different from that listed on the title page of this manual, then there are differences between the product described by this manual and your product.

Specifications

Resolution and Range

Optics	Resolution	Range
Linear or Single Beam	λ/512 or 1.25 nm (0.5 μin)	±21.2 m (69.6 ft)
Plane Mirror	λ/1024 or 0.625 nm (0.25 μin)	±10.6 m (34.8 ft)
High Resolution	λ/2048 or 0.3125 nm (0.125 μin)	±5.3 m (17.4 ft)
Vacuum λ = 632.991xx nm (See laser head specifications for exact values)		

Maximum Axis Velocity (Slew Rate)

	Laser Head		
Optics	**Agilent 5517A**	**Agilent 5517B**	**Agilent 5517C**
Linear or Single Beam	406 mm (16 in)/sec	508 mm (20 in)/sec	711 mm (28 in)/sec
Plane Mirror	203 mm (8 in)/sec	254 mm (10 in)/sec	356 mm (14 in)/sec
High Resolution	102 mm (4 in)/sec	127 mm (5 in)/sec	178 mm (7 in)/sec

The 10897B board will accept future laser head upgrades up to 1400 mm/sec with linear optics, 700 mm/sec with plane mirror optics, and 350 mm/sec with high resolution optics.

Position Outputs

This section first describes the specifications of the VMEbus position outputs and then describes the separate P2 connector Hardware Position Output specifications.

VMEbus position output

Data Format

Units: fractions of a wavelength
2's-Complement: choose any 32 of 35 bits to read
Positive Logic
Least Significant Bit (or one count) equals resolution

Data Rate Over Backplane (minimum)

> 100 kHz

Sample Data Age

Fixed: The following explanation assumes that a user has synchronized their sample with the falling edge of the 10 MHz clock. After such a sample, the value in the VMEbus position register will reflect an actual position that occurred *X* ns before the sample operation was initiated, where:

- X = 790 ns when the Sample Delay Register Bit = 1*
- X = 290 ns when the Sample Delay Register Bit = 0*

* The ability to program this sample delay is discussed in the Sample Delay Register sections of Chapter 4 in this manual.

NOTE

The availability of the second choice for *X* above makes it easier to capture the actual position at the exact instant of the sample, and place it into the position register. To use this capability, the user must add exactly 290 ns of delay between the moment of sampling and the instant in time when the hardware sample line is asserted.

Variable (typical):

< 800 ps over the full power supply specification range, and

< 40 ps/°C

Sample Delay: The following explanation assumes that a user has synchronized their sample with the falling edge of the 10 MHz clock. Because of the delay in the sample path, the earliest time that the position register may be read after a sample depends on the choice made for the appropriate Sample Delay Register* bit.

When the Sample Delay Register Bit = 1*,
the position register may be read 100 ns
after the sample line is asserted.

When the Sample Delay Register Bit = 0*,
the position register may be read 600 ns
after the sample line is asserted.

* The ability to program this sample delay is discussed in the Sample Delay Register sections of Chapter 4 in this manual.

VME Position Output Timing and the Sample Delay Register: As the machine moves, the laser receiver constantly provides position information to the Agilent 10897B board. Asserting the ~sample signal tells the board to capture a specific reading. However, because the data path and the sample path have different lengths, the value captured will represent where the machine was at some time before ~sample was asserted. The ~sample assertion to VMEbus read * time limit selection is made via the Sample Delay Register.

Each one of six of the Sample Delay Register's bits controls ~sample-to- VMEbus read * time limit for one of the 10897B's six Position Registers. The register has no effect on the P2 connector hardware position output data. Refer to the VMEbus Position Output Timing and Sample Delay Register diagram below as you read the following information.

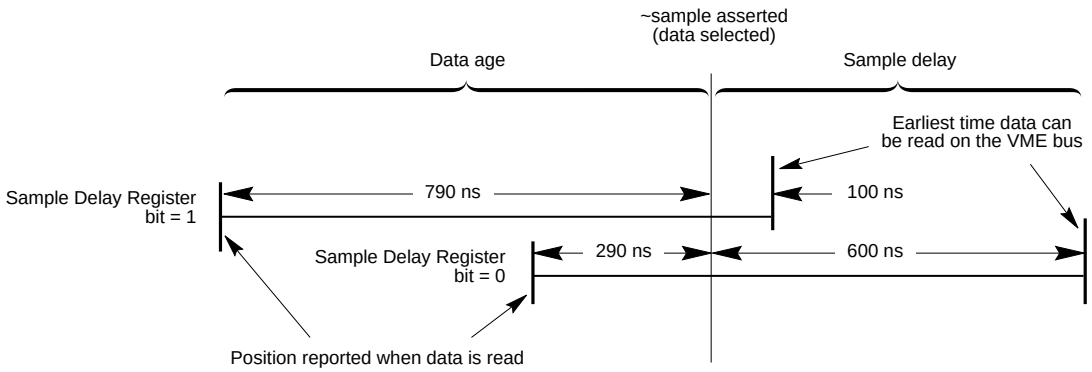
If the Sample Delay Register value for any Position register is "1" (X = Data age = 790 ns), data can be available on the VMEbus as soon as 100 ns after ~sample is asserted.

If the Sample Delay Register value is "0" (X = Data age = 290 ns), data can be available on the VMEbus as 600 ns after ~sample is asserted.

In this manual, "data age" refers to the age of the position data at the time ~sample is asserted. You cannot read this data until some later time.

In both cases (sample delay register = 0, and sample delay register = 1), the data is 890 ns old at the time it becomes available to read. This age might be called the "users data age".

When the sample delay register bit = 0, the position value read is closer to the actual position of the stage at the time ~sample is asserted. When the sample delay register bit = 1, the position data may be read soon after ~sample is asserted, or the auto sample function may be used. See the description of the Position and Velocity Registers in Chapter 4 for more information about the auto-sample function. Select the timing delay that meets your needs.



VMEbus Position Output Timing and Sample Delay Register

P2 Connector Hardware Position Output

Data Format

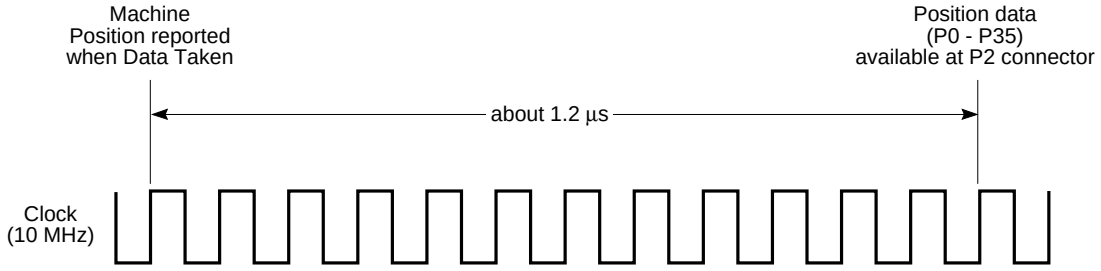
Units: fractions of a wavelength
2's Complement: 36-bit parallel binary
Positive Logic
Least Significant Bit (or one count) equals resolution

Data Update Rate

All Laser Heads: 10 MHz
(Hardware included to synchronize to slower clocks)

Data Age

Fixed: If the outputs are not being held by the Output Hold line, position data at the P2 connector represents the position of the stage approximately 1.2 µs before the next rising edge of the 10 MHz Clock.



Variable (typical):

< 800 ps over the full power supply specification range, and

< 40 ps/°C

Backplane I/O Characteristics

All backplane I/O signals are TTL-compatible. Refer to Chapter 2 of this manual for more backplane signal information.

Power Requirements

- 5 Vdc +0.25 V / -0.125 V at less than 3.5 A.
- +12 Vdc ±0.5 V at less than 0.1 A
- -12 Vdc ±0.5 V at less than 0.025 A

Weight

0.45 kg (1 lb)

Cooling Requirements

19 linear meters (60 linear feet) per minute for 0–40 °C
76 linear meters (250 linear feet) per minute minimum for 0–55 °C operation.

VME Compliance

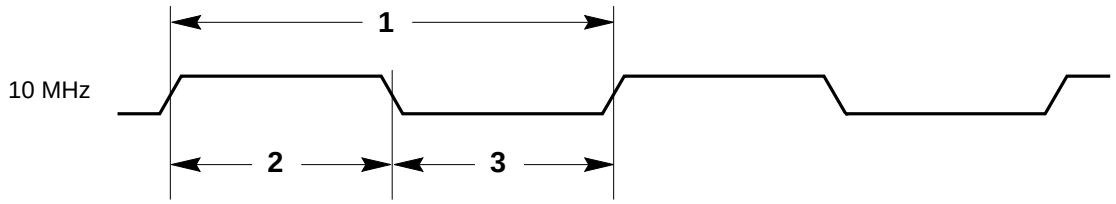
- Complies with VME Spec Rev. C.1
- 6U size
- A16 Data Transfer Cycles
- A24 Data Transfer Cycles
- D16 Data Transfer Cycles
- D32 Data Transfer Cycles
- D08(O) Interrupt acknowledge cycles

Timing Data

The following four pages provide information about backplane signal timing. This information is needed to design complementary servo circuitry for the Agilent 10897B. Eight different types of timing functions (and their various modes of operation) are covered for various backplane signals, they are:

- Clock Timing
- Position Output Timing
- Asynchronous Mode Timing
- Window and Error Output Timing
- Output Timing
- Output Hold Timing
- Position Reset Timing
- Force Zero Timing

Clock Timing



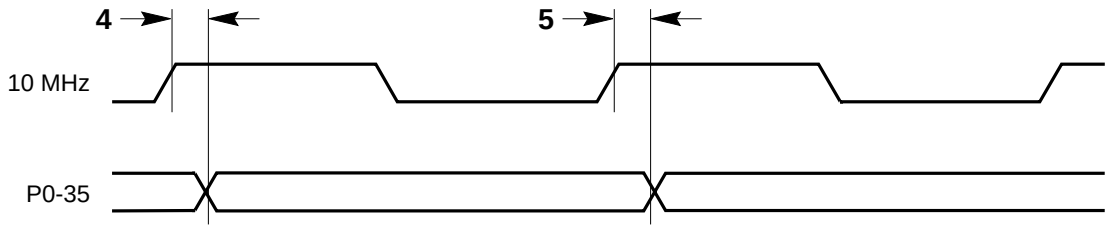
Clock Modes 1 and 3

Ref	Parameter	Min	Max
1	Clock Period	95 ns	105 ns
2	Clock High	35 ns	
3	Clock Low	35 ns	

Clock Mode 2

Ref	Parameter	Min	Max
1	Clock Period (Average)	99.99 ns	100.01 ns
2	Clock High	45 ns	55 ns
3	Clock Low	45 ns	55 ns

Position Output Timing



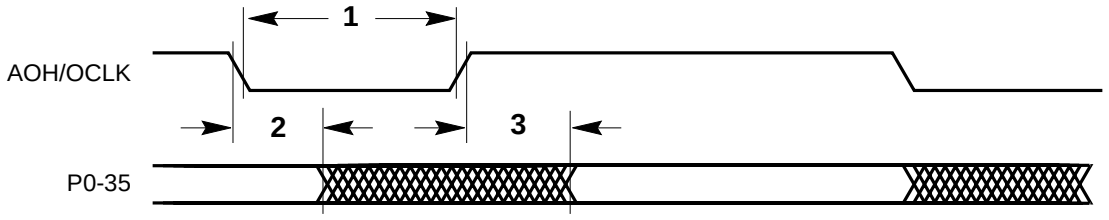
Clock Modes 1 and 3

Ref	Parameter	Min	Max
4	Clock to Position Output Valid		28 ns
5	Position Output Hold Time	4 ns	

Clock Mode 2

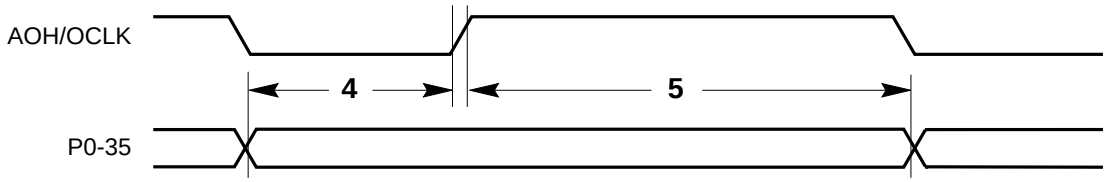
Ref	Parameter	Min	Max
4	Clock to Position Output Valid		25 ns
5	Position Output Hold Time	0 ns	

Asynchronous Mode Timing



Async Mode 1 Timing (Asynchronous Hold Input Mode)

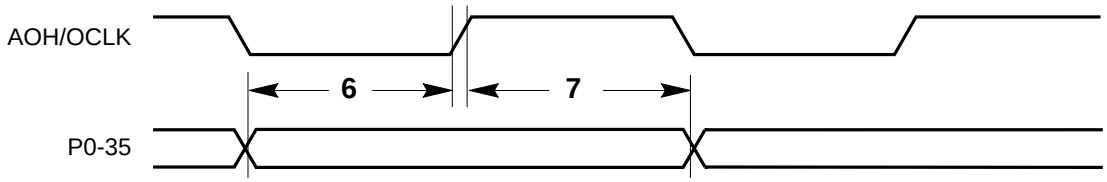
Ref	Parameter	Min	Max
1	AOH/OCLK low	120 ns	
2	AOH/OCLK low to output invalid	100 ns	
3	AOH/OCLK high to output valid		120 ns



Async Mode 2 Timing (Output Clock Mode < 10 MHz Output Rate)

Ref	Parameter	Min	Max
4	Output Valid to AOH/OCLK High	85 ns	
5	AOH/OHC high to Outputs Change	**	

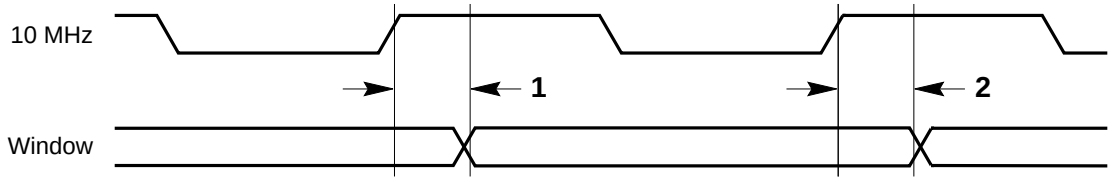
** [(100*N)-20] ns, where ns = value loaded in the Output Hold and Rate Control Register.



Async Mode 3 Timing (Output Clock Mode at 10 MHz Output Rate)

Ref	Parameter	Min	Max
6	Output Valid to AOH/OCLK High	35 ns	
7	AOH/OHC high to Outputs Change	33 ns	

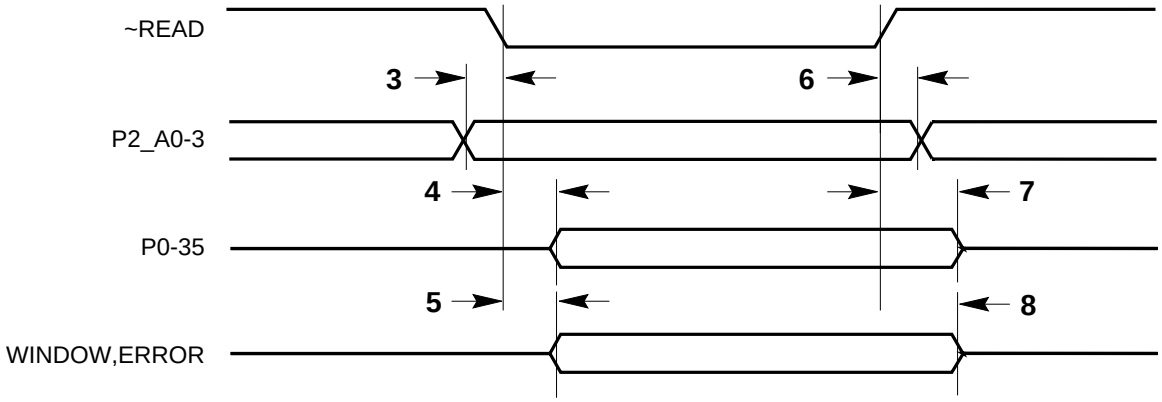
Window and Error Output Timing



Window and Error Output Timing

Ref	Parameter	Min	Max
1	Clock to WINDOW Output Valid		65 ns
2	WINDOW Output Hold from Clock	4 ns	

Output Timing

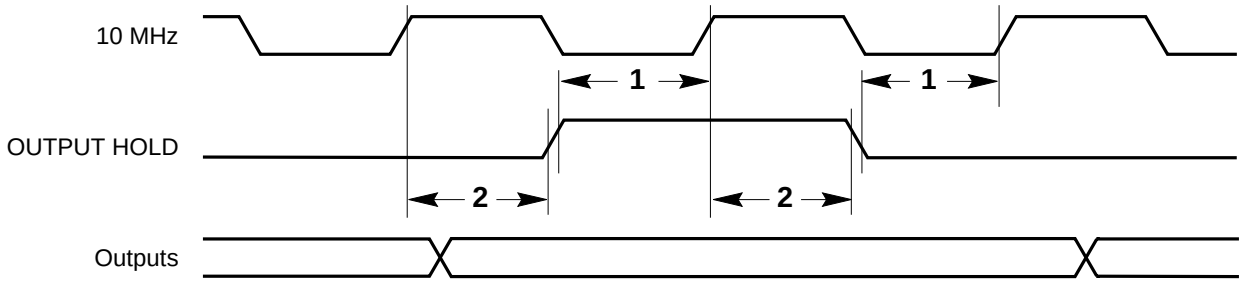


Output Timing

Ref	Parameter	Min	Max
3	Address Stable to ~READ Low *	18 ns	
4	~READ Low to Output Valid		27 ns
5	~READ Low to WINDOW or ERROR Outputs Valid **		17 ns
6	Address Hold from ~READ *	-3 ns	
7	Output Hold from ~READ	4 ns	
8	WINDOW and ERROR Output hold from ~READ **	4 ns	

* Bus Mode Only
** Window or Error Modes 3 and 7 only

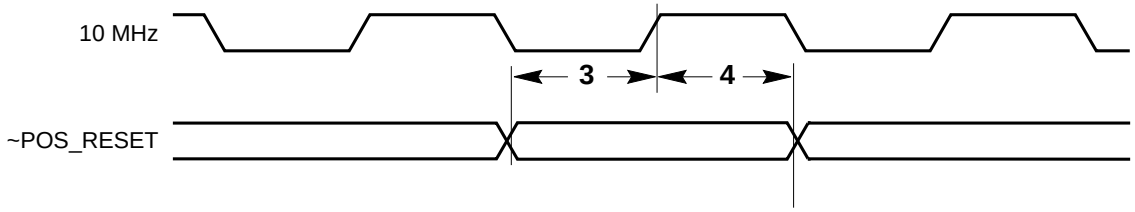
Output Hold Timing



Output Hold Timing

Ref	Parameter	Min	Max
1	OUPTUT HOLD Input to Clock Setup Time	20 ns	
2	OUPTUT HOLD Input to Clock Hold Time	0 ns	

Position Reset Timing

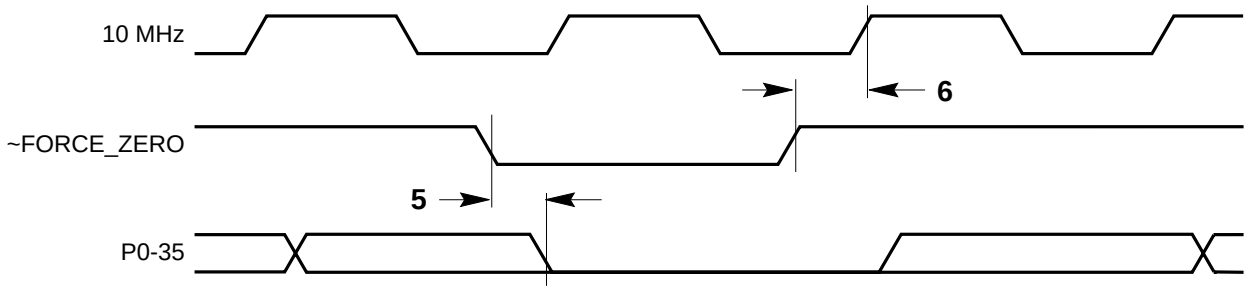


Position Reset Timing

Ref	Parameter	Min	Max
3	~POS_RESET Input to Clock Setup Time *	20 ns	
4	~POS_RESET Input to Clock Hold Time *	0 ns	

* ~POS_RESET may be asynchronous provided it is held active for at least 120 ns.

Force Zero Timing



Force Zero Timing

Ref	Parameter	Min	Max
5	~FORCE_ZERO Low to Position Outputs Zero		50 ns
6	~FORCE_ZERO High to Clock Setup Time	24 ns	

2

Installation

Introduction

This chapter provides information about unpacking, inspection, repacking, storage, and installation of the Agilent 10897B High Resolution VMEbus Laser Axis Board.

The Agilent 10897B High Resolution VMEbus Laser Axis Board is shipped with the following items:

- Operating and Service manual if Option AV4 was ordered.
- An Axis Interconnect Cable that corresponds to Option 002 through 007 if a corresponding option was ordered.

Unpacking and Inspection

CAUTION

Always use Electrostatic Discharge (ESD) precautions when handling the Agilent 10897B board outside of its protective packing materials.

If the shipping carton is damaged, ask that the carrier's agent be present when the product is unpacked. Inspect the product for damage. If the product is damaged or fails to meet electrical specifications, notify the carrier and the nearest Agilent Technologies Sales and Service office immediately.

Retain the shipping carton and padding material for the carrier's inspection. The Sales and Service office will arrange for the repair and replacement of your product without waiting for the claim against the carrier to be settled.

Storage and Shipment

To protect the board during storage or shipment, good antistatic commercial packing methods should be used. Reliable commercial packing and shipping companies have the facilities and materials to adequately repack a product.

NOTE

Before returning a product, contact the nearest Agilent Technologies Sales and Service office for instructions.

Conditions during storage and shipment should normally be limited as follows:

- Minimum temperature: -40 °C (-40 °F).
- Maximum temperature: +75 °C (+167 °F).

Installation

Proper installation of the Agilent 10897B board consists of the following steps:

CAUTION

Ensure the slot is intended for the Agilent 10897B board because the board could be damaged if it is installed in the wrong slot. The I/O on the outer rows of the slot's P2 connector must be compatible with the 10897B board's P2 pinout. Refer to the compatibility section in Chapter 1.

1. Set the address with switches S1 and S2 as described later in this chapter.
2. Ensure that correct power and cooling will be supplied to the board before it is powered on for the first time. (Refer to Specifications in Chapter 1 for more details.) The 10897B board receives its power from the VME backplane.
3. Carefully slide the board into the desired slot of your VMEbus cardcage and ensure that the P1 and P2 connectors are fully seated without binding or jamming.
4. Ensure that the correct front- or rear-panel signal connections are present (Refer to the Input and Output Connectors section of this chapter for more details.).

Input and Output Connectors

Front Panel I/O

Meas 1 and Meas 2/Ref (4-pin circular female connector)

These connectors receive laser measurement signals from either the laser head reference output or laser measurement receivers. The +15V and +15V RETURN are bused between these measurement input connectors and the Multi-Axis Interconnect connector, allowing +15-volt power distribution from one source to all measurement receivers in a system.

Multi-Axis Interconnect (16-pin ribbon connector)

This connector contains the +15V and +15V RETURN signals as well as the four lines designated as “Common Laser Signals.” The 10897B board can be programmed to drive any of these lines with the signals from either of the Measurement Input connectors. The 10897B board may also be programmed to receive its measurement signals from its Measurement Input connectors, any of the four common laser signal lines, or the external measurement inputs on P2. This capability is described in Section 4, in the discussion of the Laser Source Control Register.

Backplane Signal Usage

The 10897B board uses all pins on P1 and the center row of pins on P2 as per the VMEbus Rev C.1 specification. The outer rows of P2 are used by the 10897B board for the signals described below and listed on a following page. All backplane I/O signals are TTL-compatible. Input leakage and output drive current values (in mA) appear at the end of each of the following signal description paragraphs.

NOTE

Throughout this manual, the ~ is used to indicate negative true signals.

P0–P35 Outputs

P0–P35 is a 36-bit real time tri-state position output which, when enabled, will reflect the value of the 35-bit position counter minus the 35-bit offset register.

EXT Measure, EXT Reference Inputs

The Ext. Measure and Ext. Reference signals are an alternate source of laser measurement signals. These are enabled by writing the appropriate values into the Laser Source Control register.

Error Output

The Error signal is a status output that can be programmed via the P2 Error Mask Register to indicate the presence of any of the seven error indicators. This output can be programmed via the Output Control Register to operate as an open collector, TTL, or tri-state output.

Window Output

The Window signal is an output signal indicating that the magnitude of the position output lines P0-35 is within the range specified by the window mask register. This output can be programmed via the Output Control Register to operate as an open collector, TTL, or tri-state output.

Force Zero Input

The Force Zero input, when pulled low, forces the 36 output lines (P0–P35) to zero.

~Sample 1-4 Inputs

The ~Sample inputs cause the position counter to be latched into their respective position holding registers. This occurs when the respective ~Sample signal makes a high to low transition. The ~Sample 1 and ~Sample 2 inputs may also be programmed via the General Control/Status Register to simultaneously sample the Velocity 1 and Velocity 2 registers respectively.

~Position Reset Input

The ~Position Reset input, when pulled low, causes the position counter to either be zeroed or set to the value in the offset register depending on the state of the preset mode bit in the general control register.

Output Hold Input/Output

The Output Hold Input, when pulled high, causes the 36-bit position output to hold its current value.

The 10897B board can also be programmed via the Output Control Register to drive this line in two ways:

- By using the AOH/OCLK line as an asynchronous hold input (see Output Control Register: Async Mode section). Here the user drives the AOH/OCLK line which then causes the Output Hold line to be driven by the 10897B synchronously with its 10 MHz clock.
- By using the internal divide-by-N feature (see Output Hold and Rate Control Register section). In this mode, the 10897B board “unholds” for one 100 ns period every N 100 ns periods, where N is programmed to be 1 through 64. Several 10897B boards can be tied together in this mode with one 10897B board programmed as the master. This provides multiaxis synchronous output rates between 156.25 kHz and 10 MHz.

~Read Input

The ~Read inputs are programmed via the Output Control Register to operate in one of two modes: Bus Mode and Non Bus Mode.

In Non Bus Mode, when the ~Read input is pulled low, the 36 position output bits are enabled. When ~Read is high, the output lines will be in a high impedance state. The Error and Window outputs will also be enabled by ~Read if they are programmed in the 3-state mode via the Output Control Register.

Bus Mode operates in the same manner with the following exception: A0-3 must match the value loaded into the P2 address bits of the Output Control Register before outputs are enabled.

10 MHz Clock Input/Output

The 10 MHz Clock line can be programmed via the Output Control Register to operate as an input and/or an output. When programmed as an output, the 10897B board drives this line from a local crystal controlled source.

When programmed as an input, the 10897B board can use this line for its local clock source. This allows multiple 10897B boards to be synchronized to one 10 MHz source.

AOH/OCLK Input/Output

The AOH/OCLK signal can be programmed via the Output Control Register to operate as an asynchronous output hold input or a position output clock. When programmed as an asynchronous output hold input, an asynchronous hold signal may be applied, and the position output bits will be guaranteed stable and held within 100 ns of this input going high.

When programmed as an output clock, the position output bits can be latched into your register on the rising edge of AOH/OCLK.

A0–A3 Inputs

The A0–A3 address inputs are used as qualifiers for the ~Read input when the 10897B board is programmed in Bus Mode via the Output Control Register. In this mode, the states of A0-A3 must match the value of the address bits in the output control register for ~Read to enable the data outputs.

Table 2-1. Signal Currents

Signal	I_{ih} (mA max.)	I_{il} (mA max.)	I_{oh} (mA max.)	I_{ol} (mA max.)
P0–P35 Outputs	—	—	-0.6	8.0
EXT Measure, EXT Reference Inputs	0.02	-0.6	—	—
Error Output	—	—	-15.0	64.0
Window Output	—	—	-15.0	64.0
Force Zero Input	0.01	-0.1	—	—
~Sample 1-4 Inputs	0.01	-0.1	—	—
~Position Reset Input	0.01	-0.1	—	—
Output Hold Input	0.01	-0.01	—	—
~Read Input	0.02	-0.6	—	—
10 MHz Clock Input/Output	0.07	-0.07	-15.0	64.0
AOH/OCLK Input/Output	0.07	-0.07	-15.0	64.0
A0–A3 Inputs	0.02	-0.6	—	—

P2 Pin Assignments

Pin assignments for the outer two rows of P2 are shown in Table 2-2.

NOTE

Pin A1 has a square pad.

Table 2-2. P2 Pin Assignments

Pin	Row A	Row C
1	Ext. Measure In	Ground
2	Ext. Reference In	Ground
3	AOH/OCLK, In/Out	Ground
4	Error Out	~Sample 1 In
5	Window Out	~Sample 2 In
6	~Force Zero In	~Sample 3 In
7	~Position Reset In	~Sample 4 In
8	~Read In	Output Hold
9	10 MHz Clock, In/Out	Ground
10	P0 Out	Ground
11	P2 Out	P1 Out
12	P4 Out	P3 Out
13	P6 Out	P5 Out
14	Ground	P7 Out
15	P9 Out	P8 Out
16	P11 Out	P10 Out
17	P13 Out	P12 Out
18	P15 Out	P14 Out
19	P16 Out	Ground
20	P18 Out	P17 Out
21	P20 Out	P19 Out
22	P22 Out	P21 Out
23	Ground	P23 Out
24	P25 Out	P24 Out
25	P27 Out	P26 Out
26	P29 Out	P28 Out
27	P31 Out	P30 Out
28	P32 Out	Ground
29	P34 Out	P33 Out
30	A0 In	P35 Out
31	A2 In	A1 In
32	Ground	A3 In

Address Switches (S1, S2)

The Agilent 10897B board's base address location can be set on any 512-byte boundary in A16 or A24 address space. The rightmost position of S1 (Figure 2-1 below) determines the address space: down for A16 and up for A24.

In A16 mode, the remaining positions on S1 will determine the A16 base address locations with the leftmost position corresponding to the MSB (A15). S2 is not used in A16 mode.

In A24 mode (rightmost position of S1 up), both S2 and the seven leftmost positions of S1 are used in determining the base address location, with the leftmost position of S2 corresponding to A23. For example, Figure 2-1 shows a board configured in A16 mode with a base address of $0400.

Address Switches (S1, S2)

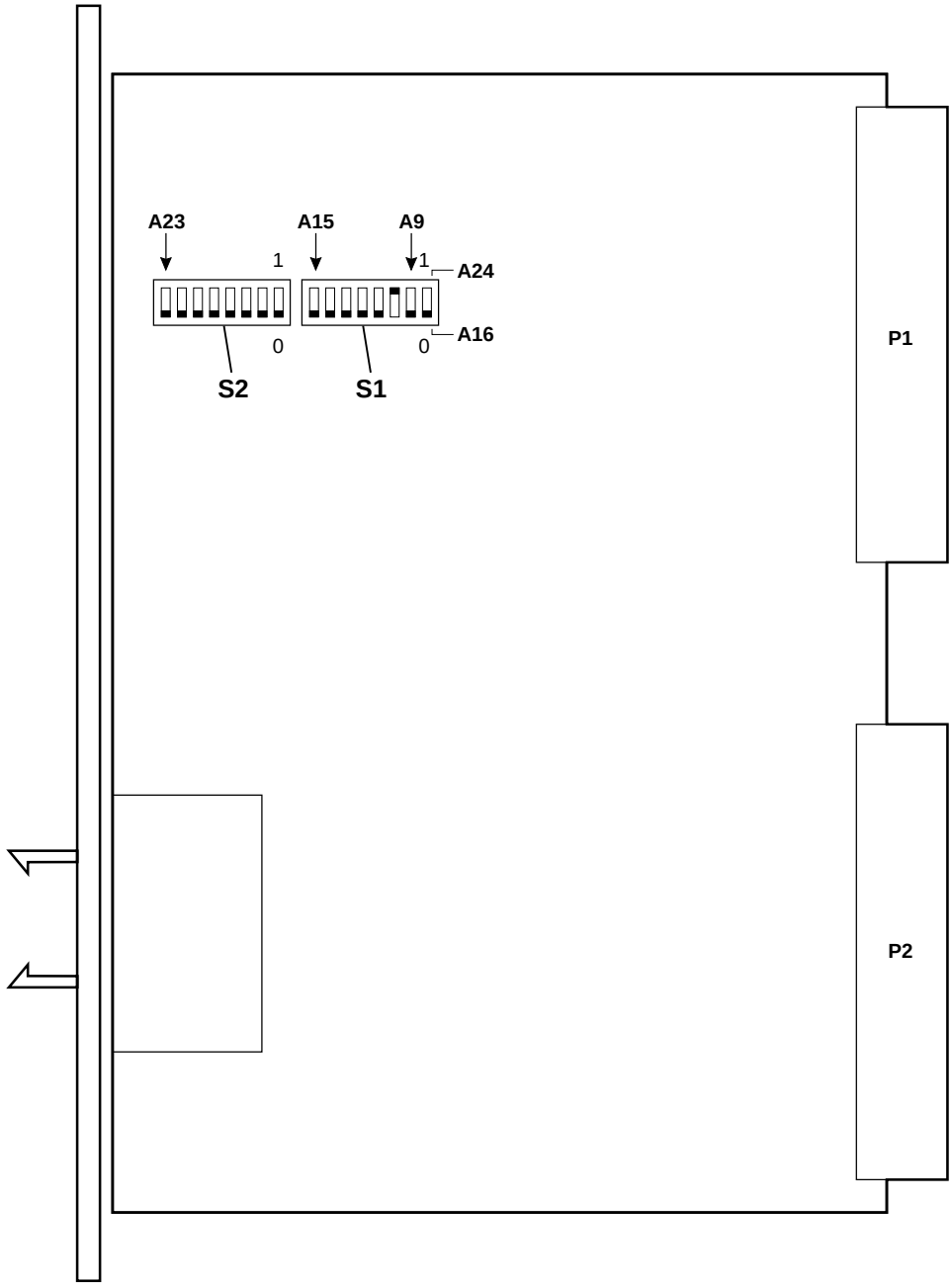


Figure 2-1. Agilent 10897B Board Address Switches

Example VMEbus Laser System Block Diagram

Figure 2-2 illustrates this board's operation in a complete laser measurement/control system. Alternate configurations that do not use custom P2 wiring are also possible. A VMEbus controller having access to the position register through the standard lines on P1 and P2 can execute a servo algorithm, and output to a DAC output board. In addition, the real-time position output lines are driven by tri-state buffers, allowing parallel connection of multiple axis boards to the same custom servo board.

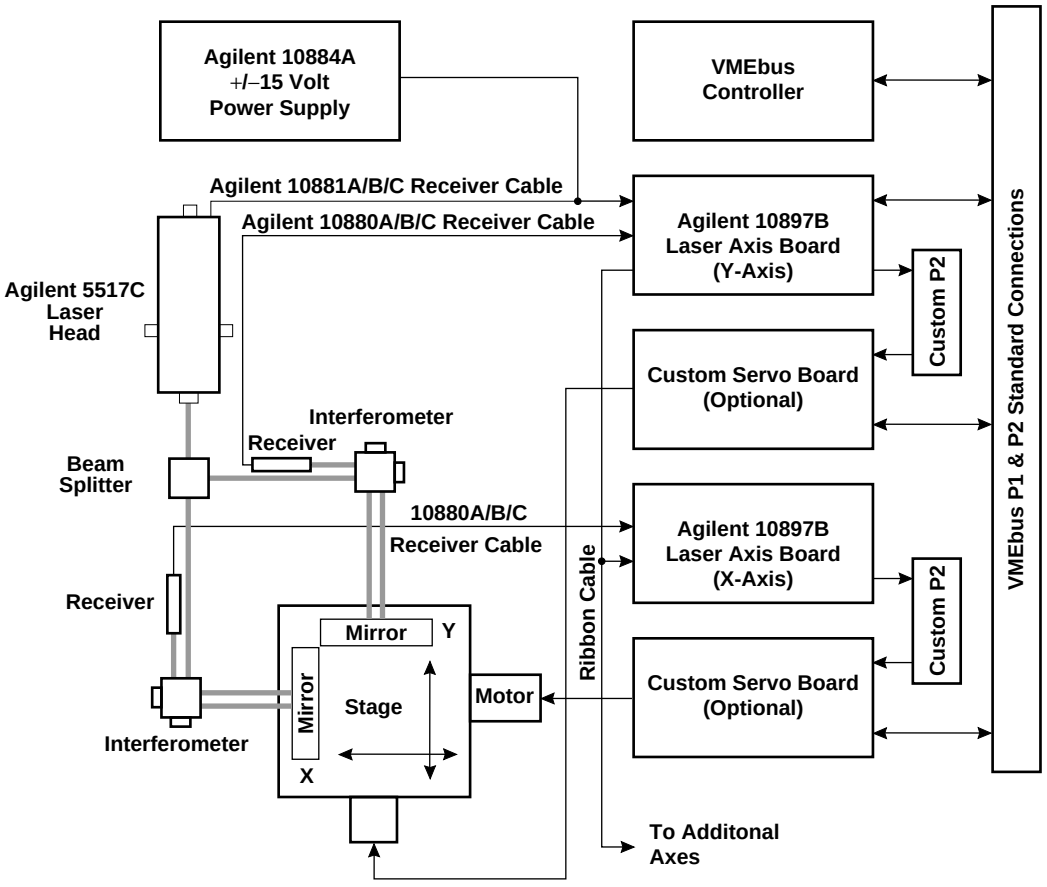


Figure 2-2. Example VMEbus Laser System Block Diagram

Example VMEbus Laser System Block Diagram

3

Getting Started

Basics

Your laser interferometer positioning system is a set of optics, electronics, and electro-optical products. This chapter will give you the information you need to quickly set up your laser system with the Agilent 10897B High Resolution Laser Axis Board.

A One-Axis Example for Simplicity

Each axis of a laser positioning system is set up, aligned, and operated in essentially the same way. However, you may need to configure the Agilent 10897B board and interfaces differently for multiaxis use. These details are covered in the multiaxis section after the single axis examples.

Basic Steps Apply to All Laser Systems

Specific products (identified by Agilent model number) are used in the example, but the installation and operation of other products are similar.

The example shows the use of VME electronics (with the 10897B board) and a linear interferometer. If you are using a different interferometer, you may need to refer to the Laser and Optics Users Manual (Agilent P/N 05517-90045) for more details on optical alignment.

Agilent Laser Interferometer Positioning Systems at a Glance

Figure 3-1 shows the components of a single-axis Agilent laser system using the 10897B board and a linear interferometer, but the system configuration is the same for all types of interferometers. Refer to the Laser and Optics Users Manual for more details.

The laser positioning system requires a controller to control the 10897B board and provide a display of the distance measured. Some VME card cages have a built-in PC. Others use a controller on a VME card or have an external controller.

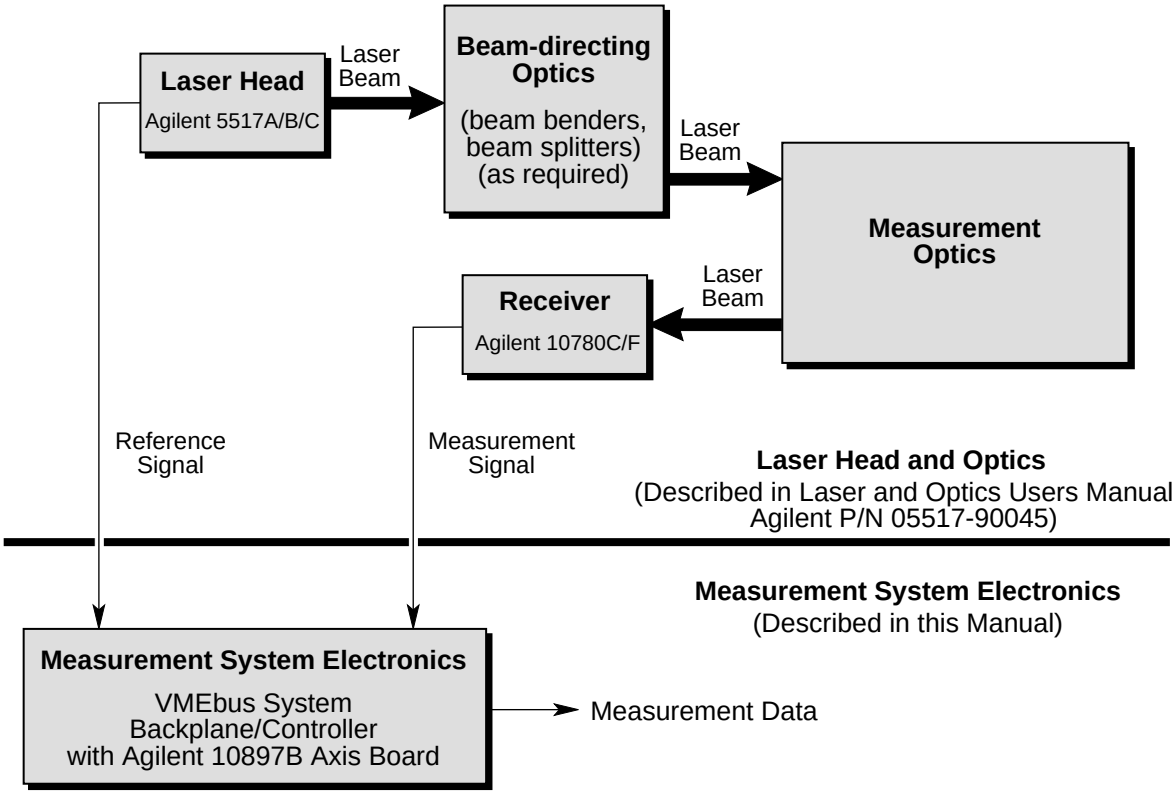


Figure 3-1. Typical Single-Axis Agilent Laser Interferometer Positioning System Using the Agilent 10897B Board

System Setup Steps

The major steps in system setup are:

1 Connect the system electronics
- Install the Agilent 10897B board in the VME backplane
- Install the controller in the VME backplane
- Install the laser head and receiver
- Connect the cables from laser head and receiver to the 10897B board

2 Install and align the optics
- Install the optics
- Align the beam from the laser head parallel to the optics motion
- Align the optics and receiver so the beam enters the receiver lens throughout the entire range of motion

3 Program the 10897B board registers

Making a measurement requires the software to be running on the controller to display measurement results. Because there are so many choices for VME backplanes, controllers, and operating systems, the information in the example describes how to configure the 10897B board registers for typical single-axis applications. You will need to translate this information into commands for the particular controller you are using. Additional information is included for multiaxis operation later in this chapter.

Setting Up the System Electronics

WARNING **UNPLUG THE POWER CORDS TO PREVENT PERSONAL INJURY AND DAMAGE TO THE ELECTRONICS.**

Installing the Agilent 10897B Board in the VME Backplane

1. Unplug the VME backplane power cord.
2. Set the 10897B board's address switches to point to a 512-byte area in A16 or A24 address space that is not used by any other board in the VME backplane. (In a multiaxis system each 10897B board must have its own unique address space.)

CAUTION **Ensure the slot is intended for the 10897B board. The 10897B board could be damaged if it is installed in the wrong slot. The I/O on the outer rows of the P2 connector must be compatible with the 10897B board's P2 connector pinout. Refer to the Compatibility section in Chapter 1.**

3. Install the 10897B board in the VME backplane.
4. Plug in the VME backplane power cord, but leave the VME power off.

Installing the Controller

Install your controller in the VME backplane.

Installing the Laser Head and Receiver

Place the Laser Head and Receiver in convenient locations. You may want to secure them in position.

Connecting the Electronics Cables

Refer to Figure 3-2 when performing these steps.

1 Connect the largest connector on the Agilent 10881(A,B,C,D,E,F) cable to the Laser Head. Connect the smallest connector to the Reference connector on the 10897B board.

2 Connect the remaining connector on the 10881(A,B,C,D,E,F) cable to the ±15 Vdc power supply (Agilent 10884A Power Supply or equivalent).

3 Connect the Agilent 10880A,B,C receiver cable to the receiver and to the 10897B board.

4 Connect the ac line cord to the Agilent 10884A Power Supply's input connector (or the input of the power supply being used), but do not connect the power supply to an operating ac line outlet.

NOTE The 10884A Power Supply has no power switch. As soon as it is plugged in it will provide output power and its LED indicator will light.

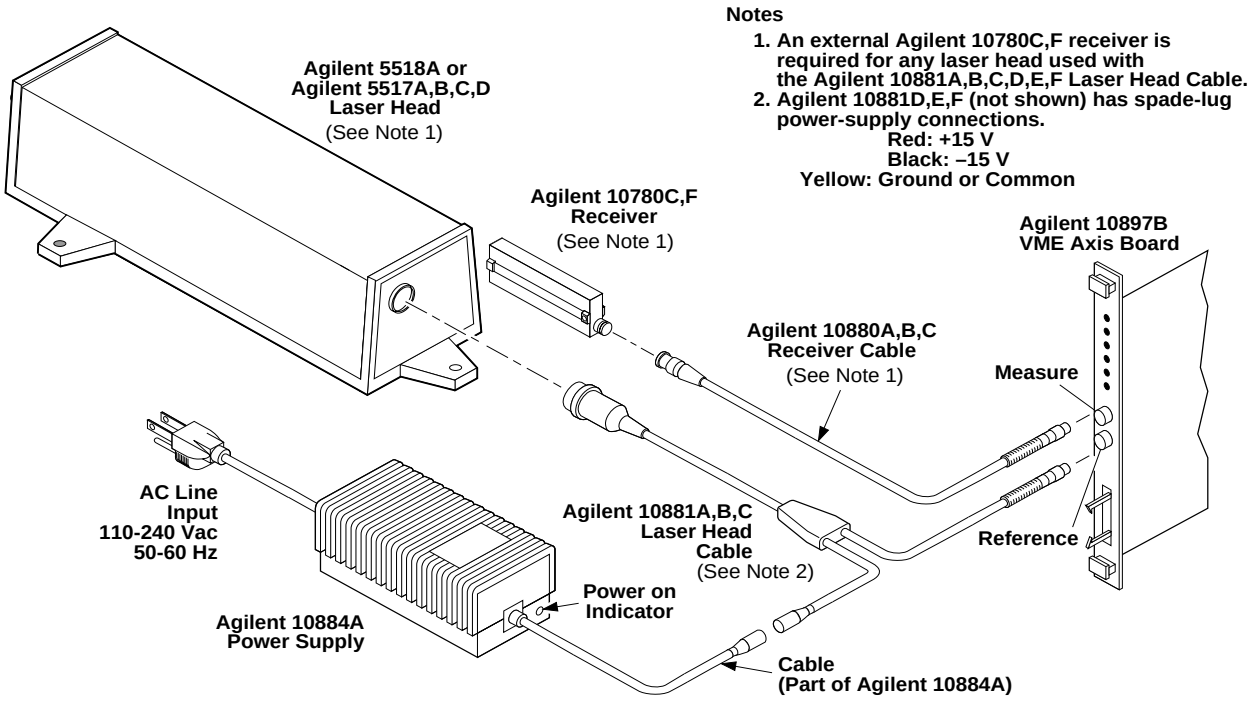

Notes
1. An external Agilent 10780C,F receiver is required for any laser head used with the Agilent 10881A,B,C,D,E,F Laser Head Cable.
2. Agilent 10881D,E,F (not shown) has spade-lug power-supply connections.
Red: +15 V
Black: –15 V
Yellow: Ground or Common
Agilent 5518A or Agilent 5517A,B,C,D Laser Head
(See Note 1)
Agilent 10780C,F Receiver
(See Note 1)
Agilent 10897B VME Axis Board
Agilent 10880A,B,C Receiver Cable
(See Note 1)
Measure
AC Line Input 110-240 Vac 50-60 Hz
Agilent 10881A,B,C Laser Head Cable
(See Note 2)
Reference
Power on Indicator
Agilent 10884A Power Supply
Cable (Part of Agilent 10884A)

Figure 3-2. Installation of Laser System Cables

Starting the System

1 Turn on the power to your VME backplane.

2 Plug the ac line cord for the laser head power supply into an operating ac line outlet. The laser head should emit a red laser beam within 45 seconds after receiving power. The laser head requires a four- to ten-minute warm-up period to stabilize its output before a measurement can be made.

WARNING **DO NOT STARE DIRECTLY INTO THE LASER BEAM (OR ITS REFLECTION FROM A POLISHED SURFACE) OR EYE DAMAGE COULD RESULT.**

Aligning the Optics

The laser head, optics, and receiver must be aligned so the laser beam returning from the optics enters the receiver lens.

1 Set the laser head on a stable surface and point the beam in the direction along which you intend to move the optics.

2 Place the interferometer in the laser beam path so its input aperture is perpendicular (normal) to the beam. You may need to fasten the interferometer in place with a clamping fixture.

3 Place the reflector in the laser beam line coming from the interferometer. Adjust the reflector to reflect the beam back into the interferometer.

4 Place the receiver parallel to the laser beam from the laser head to the interferometer with the receiver's lens facing the interferometer. Fasten the receiver in place with a fixture or clamp.

5 Adjust the reflector and receiver so the return beam enters the receiver lens. When the Laser Head's "Laser Ready" indicator comes on, the receiver's green LED will light when the beam alignment is satisfactory.

6 Block the beam from the interferometer to the receiver. The green LED on the receiver should go out. Unblock the beam and the green LED should light again. If this happens, alignment is complete and you can skip step 7 of this procedure.

If the receiver's green LED stays on when the beam from the interferometer is blocked, the receiver gain is too high. Go to the next step.

7 With the beam blocked, turn the receiver's gain adjustment control until the LED goes out. When the beam is unblocked, the LED should light again, indicating that the optics are aligned properly. If the green LED does not light, repeat steps 5 through 7 until it does light.

Programming the Agilent 10897B Registers

To make a measurement:

- the electronics must be connected and operating,
- the laser beam must be aligned, and
- a software program which configures the Agilent 10897B board for the particular application and makes the required measurements must be running in the controller.

Listed below are the steps that you must complete to configure the 10897B board and interface for typical applications. Only register values are given; you must translate these into the program language your controller uses. The examples are for a single axis. The procedure for a three-axis system follows the single-axis examples.

Example 1: Reading Position Over the VME Bus

1 The example uses a base address of $1000 in A16 space (refer to Figures 2-1 and 3-3).

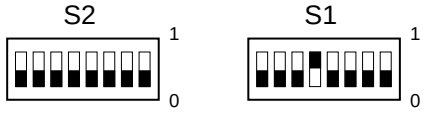


Figure 3-3. Address Switch Setting for $1000 Address

2 Using word transfers, write the following data to the operating registers indicated:

Register Name	Extended Address	Data Xfr Size	Data (Hex)
1. General Control/Status	$1000	Word	$0000
2. Laser Source Control	$1004	Word	$0001
3. Output Control	$1008	Word	$0000
4. Sample Delay	$109A	Word	$00FF
5. Sample Mode & Mask	$109E	Word	$0000
6. IRQ Error Mask	$10A6	Word	$007F
7. Overflow Level & Output Format	$10BE	Word	$0000
8. Filter Control	$10BA	Word	$0010
9. Wait > 1 msec	—	—	—
10. Error Status & Reset	$10B2 $10B2	Word	$007F $0000
11. Command Register	$100C	Word	$0100

The first ten steps complete the initialization of the 10897B board. Step 11 resets the position to zero by writing to the Command Register.

The 10897B board should now be configured for reading position via the VME backplane. Because interrupts are not being used in this example, bit 11 of the General Control/Status Register must be continuously monitored. If a '1' is read from this bit position, an error has occurred and the position data may be invalid. The error condition is cleared by performing steps 8 through 11 above.

3 Read the position using the Auto Sample feature. Do this by executing a long-word read at address $1120. If you wish to execute two word reads, always read the more significant (lower address) word first because the auto-sample occurs when the most significant word is read.

Register Name	Extended Address	Data Xfr Size	Data (Hex)
12. Position Register 1	$1120	Long Word	$????????

NOTE

In the example above the sampling was done in software using the Auto Sample feature. The position and velocity registers may also be sampled by the hardware sample inputs on the P2 connector. To determine if a hardware sample has occurred, read the Sample Status Register. For example, if the ~ Sample 1 In line was asserted, this will cause the Sample Status Register bit zero to be set, indicating a sample had occurred for Position Register 1. Position Register 1 may then be read by a long-word read operation at address $1100. Note that this address is used so as not to cause an Auto Sample since the register was sampled via the hardware. Reading Position Register 1 will clear bit zero in the Sample Status Register.

Example 2: Fixed Rate Hardware Outputs

This example shows how the registers could be configured to use the P2 hardware outputs P0–P35.

1 The example uses a base address of $1000 in A16 space (refer to Figure 3-3).

2 Write the values shown to the registers indicated:

Register Name	Extended Address	Data Xfr Size	Data (Hex)
1. General Control/Status	$1000	Word	$0000
2. Laser Source Control	$1004	Word	$0001
3. Output Control	$1008	Word	$0010
4. Sample Delay	$109A	Word	$00FF
5. Sample Mode & Mask	$109E	Word	$0000
6. IRQ Error Mask	$10A6	Word	$007F
7. Overflow Level & Output Format	$10BE	Word	$0000
8. Position Offset-Sign Extend	$1088	Long Word	$00000000 §
9. Output Hold & Rate Control	$10B6	Word	N
10. Filter Control	$10BA	Word	$0010
11. Wait > 1 msec	—	—	—
12. Error Status & Reset	$10B2 $10B2	Word	$007F $0000
13. Command Register	$100C	Word	$0100

§ This is for zero offset. For an offset other than zero, write that value to this register.

This procedure causes the 10897B board to output position data at the rate 10 MHz/(N+1). N is set in step 9 as shown above, and may range from 0 to 63.

The 10897B board may be programmed to provide an output clock that can be used to clock the hardware position data. This feature can be used by writing $3010 to the Output Control Register for 10 MHz output rate, or by writing $2010 to the Output Control Register for output rates less than 10 MHz. In these cases the clock output is on the AOH/OCLK pin. Refer to the Timing Data Section in Chapter 4 for specific timing details.

Example 3: User-Controlled Hardware Outputs—Synchronous

You may synchronously control the 10897B board's hardware position output rate via the Output Hold line. Follow these steps to use this method of output control.

1 The example uses a base address of $1000 in A16 space (refer to Figure 3-3).

2 Write the values shown to the registers indicated:

Register Name	Extended Address	Data Xfr Size	Data (Hex)
1. General Control/Status	$1000	Word	$0000
2. Laser Source Control	$1004	Word	$0001
3. Output Control	$1008	Word	$C010
4. Sample Delay	$109A	Word	$00FF
5. Sample Mode & Mask	$109E	Word	$0000
6. IRQ Error Mask	$10A6	Word	$007F
7. Overflow Level & Output Format	$10BE	Word	$0000
8. Position Offset-Sign Extend	$1088	Long Word	$00000000 §
9. Output Hold & Rate Control	$10B6	Word	$0080
10. Filter Control	$10BA	Word	$0010
11. Wait > 1 msec	—	—	—
12. Error Status & Reset	$10B2 $10B2	Word	$007F $0000
13. Command Register	$100C	Word	$0100

§ This is for zero offset. For an offset other than zero, write that value to this register.

You may assert the Output Hold input when you want the hardware position outputs held. This input signal must be synchronous with the 10 MHz clock on pin P2-A9 (10 MHz Clock In/Out). Refer to the Timing Data section in Chapter 4 for timing requirements.

Example 4: User-Controlled Hardware Outputs—Asynchronous

You may asynchronously control the 10897B board's hardware position output rate via the AOH/OCLK line. Follow these steps to use this method of output control.

1 The example uses a base address of $1000 in A16 space (refer to Figure 3-3).

2 Write the values shown to the registers indicated:

Register Name	Extended Address	Data Xfr Size	Data (Hex)
1. General Control/Status	$1000	Word	$0000
2. Laser Source Control	$1004	Word	$0001
3. Output Control	$1008	Word	$1010
4. Sample Delay	$109A	Word	$00FF
5. Sample Mode & Mask	$109E	Word	$0000
6. IRQ Error Mask	$10A6	Word	$007F
7. Overflow Level & Output Format	$10BE	Word	$0000
8. Position Offset-Sign Extend	$1088	Long Word	$00000000 §
9. Output Hold & Rate Control	$10B6	Word	$0080
10. Filter Control	$10BA	Word	$0010
11. Wait > 1 msec	—	—	—
12. Error Status & Reset	$10B2 $10B2	Word	$007F $0000
13. Command Register	$100C	Word	$0100

§ This is for zero offset. For an offset other than zero, write that value to this register.

You may assert the AOH/OCLK line when you want the position outputs held. In this mode, the Output Hold line is driven by the 10897B board and you should not attempt to drive the Output Hold line. Refer to the Timing Data section in Chapter 4 for timing requirements.

Example 5: Use of Interrupts

You may program the 10897B board to generate interrupts on the VME backplane. First, the Interrupt Vector register must be loaded with the vector number that points to an interrupt service routine that the VME controller will execute to service the 10897B board. For this example, the Interrupt Vector is 255. Follow the steps below:

1 The example uses a base address of $1000 in A16 space (refer to Figure 3-3).

2 Write the values shown to the registers indicated:

Register Name	Extended Address	Data Xfr Size	Data (Hex)
1. General Control/Status	$1000	Word	$0000
2. Laser Source Control	$1004	Word	$0001
3. Output Control	$1008	Word	$0000
4. Sample Delay	$109A	Word	$00FF
5. Sample Mode & Mask	$109E	Word	$0000
6. IRQ Error Mask	$10A6	Word	$007F
7. Overflow Level & Output Format	$10BE	Word	$0000
8. Interrupt Vector	$1022	Word	$00FF
9. Filter Control	$10BA	Word	$0010
10. Wait > 1 msec	—	—	—
11. Error Status & Reset	$10B2 $10B2	Word	$007F $0000
12.Command Register	$100C	Word	$0100
13. General Control/Status	$1000	Word	$000A §

§ First write $0000 to the General Control/Status register, then write $000A to the General Control/Status register after the other registers are loaded. This prevents generating an interrupt while loading the other registers.

This configures the 10897B board to generate an interrupt, at priority level 2, when an error exists from any of the seven error sources.

It is also possible to configure the 10897B board to have an interrupt generated when one or more of the position and velocity registers have been sampled. For example, the Sample Mode and Mask register could be loaded with the value shown below to cause the 10897B board to generate an interrupt when the position 1 or velocity 1 register has been sampled.

Register Name	Extended Address	Data Xfr Size	Data (Hex)
14. Sample Mode & Mask	$109E	Word	$0041

Multiaxis Configurations

The examples above showed how to set up the Agilent 10897B board for typical single-axis applications. Most steps are the same for multiaxis applications. For most registers, the differences are self-explanatory. However, for clarity, details are provided for the following registers.

Laser Source Control Register

For most multiaxis applications the COM lines, via the front-panel 16-pin ribbon connector, will be used to bus the reference input signal and/or measurement input signals from one axis to all the others. Figure 3-4 shows an example of this for a three-axis system where two measurements are made in the Y axis to measure yaw.

The top 10897B board measures the X axis. It receives the X measure signal on the MEAS 1 input connector and the laser head reference signal on the MEAS 2 input connector. The top 10897B board then passes the reference signal to the middle 10897B board via COM 1. The middle 10897B board measures the Y axis position by receiving the Y axis measure signal on its MEAS 1 input connector. The middle 10897B board then passes the Y measure signal via COM 2 to the lower 10897B board, which receives the Y' measure signal on its MEAS 1 input connector. This allows the lower 10897B board to make a differential yaw measurement for the Y axis. The values that must be loaded into the Laser Source Control Registers for the three 10897B boards are shown in Figure 3-4.

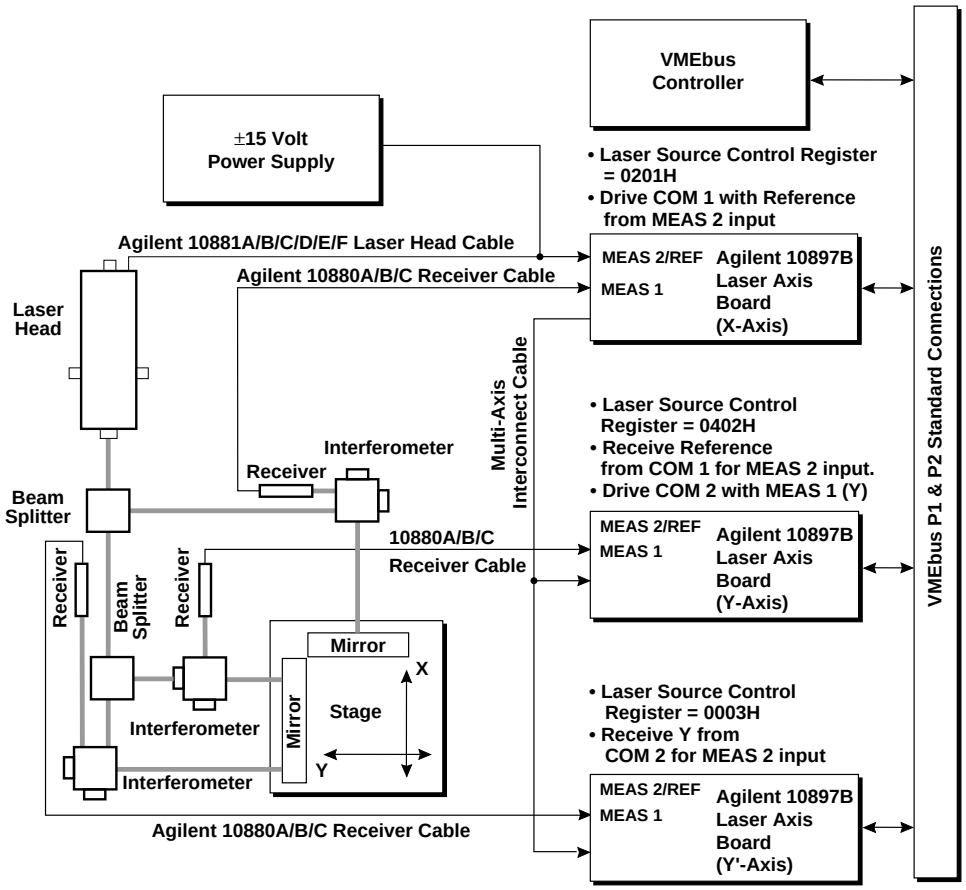


Figure 3-4. Using the COM Lines for Multiaxis Applications

Output Control Register

The Clock Mode and Async Mode features become more important for multiaxis use. Figures 3-5 and 3-6 show examples of how to use these features.

Figure 3-5 is an example of how to configure several 10897B boards so one asynchronous hold input may be used to cause all of the 36-bit position outputs to hold on the same 10 MHz clock period. Simply connecting all of the AOH/OCLK's together will not insure this. In the example shown, you simply assert the asynchronous hold input and read each 10897B board's 36-bit hardware position value, one by one, before releasing the hold input.

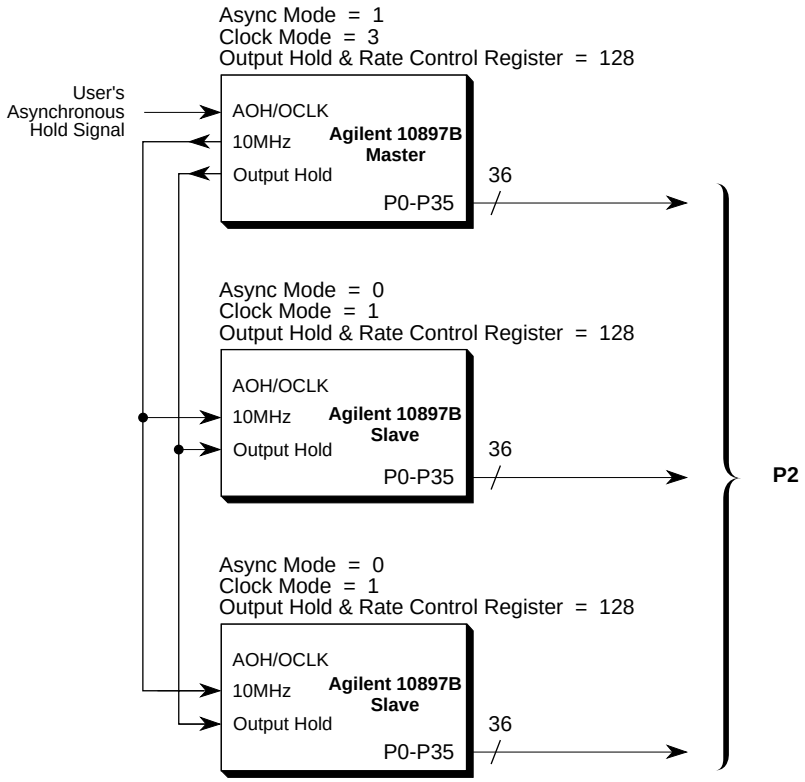


Figure 3-5. Asynchronous Hold Input for Multiaxis Applications

Figure 3-6 is an example of how to configure several 10897B boards so that the P0–P35 hardware outputs may be synchronously read at the chosen rate of 1 MHz. Here the AOH/OCLK pin is configured as an output to clock the data into your registers. In this example, each 10897B board's P0–P35 output is clocked into your register on the same 10 MHz clock, at a 1 MHz rate. Setting the Output Hold and Rate Control register to the value of 9 sets the rate to 10 MHz ÷ (9+1) = 1 MHz.

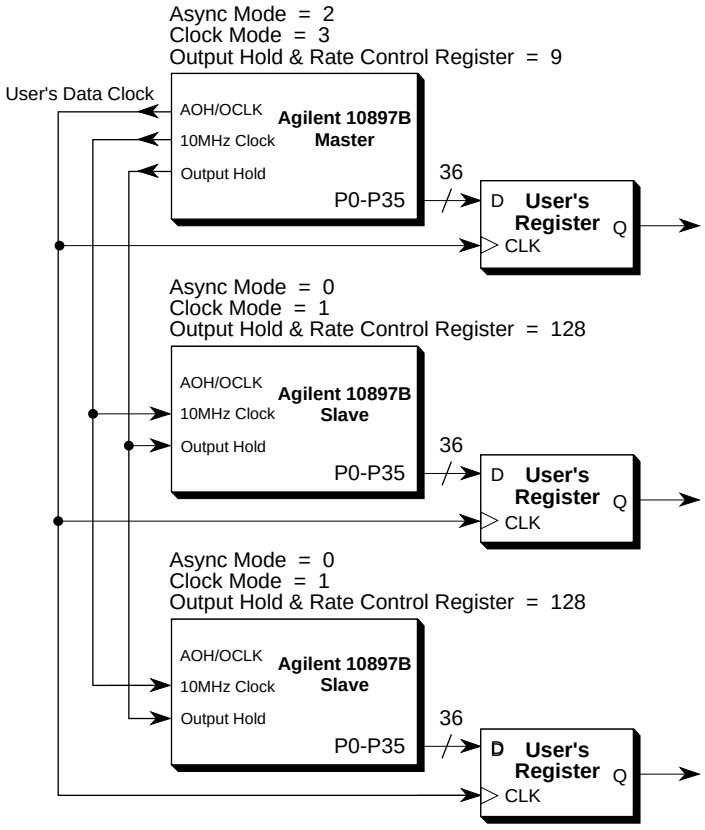


Figure 3-6. Synchronously Reading P0–P35 Outputs for Multiaxis Applications

4

Operation

Introduction

This chapter provides information about the operating features of the Agilent 10897B High Resolution VMEbus Laser Axis Board.

Data Transfer Modes

The 10897B board is compatible with the following data transfer modes:

- A16 data transfer cycles*
- A24 data transfer cycles*
- D16 data transfer cycles
- D32 data transfer cycles
- D08(O) interrupt acknowledge cycles

Address Modifier Codes

The 10897B board will respond to the following address modifier codes:

NOTE

Throughout this manual, a $ in front of a number indicates that the value is hexadecimal.

- $29 Short Non-Privileged Access*
- $2D Short Supervisory Access*
- $39 Standard Non-Privileged Data Access*
- $3D Standard Supervisory Data Access*

* The 10897B board can operate in either short or standard space as selected by the on-board address switch settings. (See Chapter 2 for addressing information.)

Indicators

The Agilent 10897B board has six front-panel LEDs (See Figure 1-1.). They consist of the following:

- Measurement A Signal Present (green)
- Measurement B Signal Present (green)

These two indicators illuminate when a signal is detected at the Measurement A Source or at the Measurement B Source, respectively. Refer to the Laser Source Control Register section under Operation for details.

- Measurement A Loss of Signal (yellow)
- Measurement B Loss of Signal (yellow)

These two indicators illuminate when the Measurement A or Measurement B Source Input circuitry has not detected a positive transition in 12.8 µsec. Refer to the Error Status and Reset Register section under Operation for details.

- Measurement Error (yellow)

This indicator illuminates if an error occurs that is unmasked by either the IRQ Error Mask Register or the P2 Error Mask Register.

- User Programmable (green)

This indicator may be turned on or off by writing to bit 7 of the General Control/Status Register. Refer to the General Control/Status Register section under the Registers section that follows.

Operation

The Agilent 10897B board is initialized (all bits in the General Control, Laser Source Control, and Output Control Registers are cleared) when the board receives a sysreset signal from the VMEbus. After this system reset, the board responds to either A16 or A24 addressing as explained in the previous chapter (A16 – A24 Base Address Switches, S1 – S2).

When powered up, the laser head takes up to ten minutes to stabilize. The General Control/Status register's Signal A and Signal B status bits indicate when the system is ready to make a measurement.

Making measurements with the board now consists of initializing various registers in accordance with the desired mode of operation appropriate for the user application. The Registers section below details operation and interpretation of each register.

Registers

The Agilent 10897B board operating registers and their address locations relative to the base address are defined in the table below. The exact address for each of these registers is determined by adding the base address (A16 or A24) to the register location.

Location	Name	Type	Size
$100 - $1FC	Position & Velocity Registers	Read Only	Long Word
$BE	Overflow Level & Output Format	Read/Write	Word
$BA	Filter Control	Read/Write	Word
$B6	Output Hold & Rate Control	Read/Write	Word
$B2	Error Status & Reset	Read/write	Word
$AA	P2 Error Mask	Read/Write	Word
$A6	IRQ Error Mask	Read/Write	Word
$A2	Sample Status	Read Only	Word
$9E	Sample Mode & Mask	Read/Write	Word
$9A	Sample Delay	Read/Write	Word
$96	Test Rate B	Read/Write	Word
$92	Test Rate A	Read/Write	Word
$8C	Clip & Window Masks	Read/Write	Long Word
$88	Position Offset - Sign Extend	Read/Write	Long Word
$84	Position Offset - LSBs	Read/Write	Long Word
$80	Position Offset - MSBs	Read/Write	Long Word
$22	Interrupt Vector	Read/Write	Word
$0C	Command Register	Write Only	Word
$08	Output Control	Read/Write	Word
$04	Laser Source Control	Read/Write	Word
$00	General Control/Status	Read/Write	Word

General Control/Status Register

The bits of the General Control/Status Register are defined as shown below.

Bit	15	14	13	12	11	10	9	8
Function	Not Used	Not Used	Signal B	Signal A	Error	Sample Pending	Pos Reset Disable	Force 0 Disable

Bit	7	6	5	4	3	2	1	0
Function	User LED	Preset Enable	Hardware Sample Mode 1	Hardware Sample Mode 0	IRQ Enable	IPL2	IPL1	IPL0

Bits 0 through 9 are read/write and are used for control; bits 10 through 15 are read only and reflect status.

Signal A and Signal B

These bits indicate the presence of the Measurement A and B signals, respectively.

Error

This bit indicates the presence of an error that is enabled by the IRQ Error Mask Register. During an IRQ service routine this bit, in conjunction with the Sampled bit, can be used to determine the cause of the interrupt.

Sample Pending

This bit indicates that a register not masked by the Sample Mode and Mask Register has been sampled since it was last read. During an IRQ service routine this bit, in conjunction with the Error bit, can be used to determine the cause of the interrupt.

Position Reset Disable

This bit, when set, will disable the hardware ~Position Reset line from resetting the position counter.

Force Zero Disable

This bit, when set, will disable the hardware ~Force Zero line from zeroing the hardware position outputs.

User LED

This bit, when set, will cause the User LED on the front panel to light.

Preset Enable

This bit controls the following events during a position reset (hardware or software): If the Preset Enable bit is zero during the position reset, the position counter will be zeroed. If it is one, the position counter will be loaded with the contents of the Offset Register.

Hardware Sample Mode 1

This bit, when set, will cause a hardware sample on ~Sample2 to simultaneously sample the velocity 2 register.

Hardware Sample Mode 0

This bit, when set, will cause a hardware sample on ~Sample1 to simultaneously sample the velocity 1 register.

IRQ Enable

This bit when set, enables VME interrupts.

IPL0–3

These bits program the interrupt level for the 10897B board.

Laser Source Control Register

Bits in the Laser Source Control register are defined as shown below. Refer to the Front Panel I/O in the Input and Output Connectors section for an explanation of the common laser signals (referred to in the table below as Com Drive).

Bit	15	14	13	12	11	10	9	8
Function	Com 4 Drive Sel 1	Com 4 Drive Sel 0	Com 3 Drive Sel 1	Com 3 Drive Sel 0	Com 2 Drive Sel 1	Com 2 Drive Sel 0	Com 1 Drive Sel 1	Com 1 Drive Sel 0

Bit	7	6	5	4	3	2	1	0
Function	not used	Meas A Sel 2	Meas A Sel 1	Meas A Sel 0	not used	Meas B Sel 2	Meas B Sel 1	Meas B Sel 0

Com Drive Bits

Any or all of the four common Laser Signal lines may be driven by either of the two input signals, Measure Input 1 and Measure Input 2. The Com Drive Select bits determine which input signal, if any, drives that Com line as shown in the table below (where x is 1, 2, 3, or 4).

Com x Drive		
Sel 1	**Sel 0**	**Operation**
0	0	Don't Drive Com x
0	1	Drive Com x With Measure Input 1
1	0	Drive Com x With Measure Input 2
1	1	Don't Drive Com x

Measurement A and B Source Select 0-2

The 10897B board requires two laser source signals to make a measurement, Measurement A and Measurement B. Normally, but not necessarily, one of these signals is the reference signal from the laser head. The two measurement inputs to the 10897B board's resolution extension circuitry are interchangeable and may be swapped to reverse the direction sense or each may be connected to

measurement receivers to obtain a differential measurement. The select values for Measurement A and B are defined as shown below.

For example, to use Meas 1 as the Measurement A source and Meas 2 as the Measurement B source without driving any Com lines, a value of $0001 would be written to the Laser Source Control register. You could also use these same measurement inputs with Com 1 driven by Meas 2 ($0201). Another 10897B board could then use Com 1 as measurement B and its front-panel Meas 1 input as measurement A by writing $0002 to its Laser Source Control register.

Meas A Sel 2	Meas A Sel 1	Meas A Sel 0	Measurement A Source
0	0	0	Meas 1
0	0	1	Meas 2/Ref
0	1	0	Com 1
0	1	1	Com 2
1	0	0	Com 3
1	0	1	Com 4
1	1	0	Test A
1	1	1	External A (P2)

Meas B Sel 2	Meas B Sel 1	Meas B Sel 0	Measurement B Source
0	0	0	Meas 1
0	0	1	Meas 2/Ref
0	1	0	Com 1
0	1	1	Com 2
1	0	0	Com 3
1	0	1	Com 4
1	1	0	Test B
1	1	1	External B (P2)

Output Control Register

Bits in the Output Control register are defined as shown below.

Bit	15	14	13	12	11	10	9	8
Function	Clock Mode Sel 1	Clock Mode Sel 0	0Async Mode Sel 1	Async Mode Sel 0	not used	WNDO Mode Sel 2	WNDO Mode Sel 1	WNDO Mode Sel 0

Bit	7	6	5	4	3	2	1	0
Function	Error Mode Sel 2	Error Mode Sel 1	Error Mode Sel 0	~Bus Mode	P2 A3	P2 A2	P2 A1	P2 A0

Clock Mode

The 10897B board requires a 10 MHz clock source for operation. This clock source may be the internal 10 MHz crystal clock or it may be externally supplied. The 10897B board may also be programmed to drive its 10 MHz clock line on P2 (10 MHz Clock, In/Out) to supply other 10897B boards (See Figure 4-1 for Clock Mode operation.) The Clock Mode bits in the Output Control Register determine the mode of operation as shown in the table below.

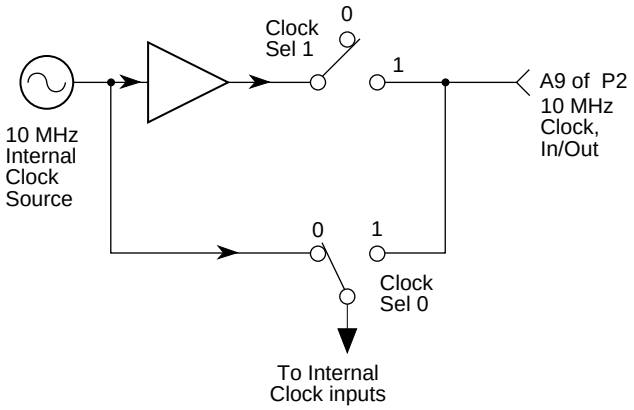


Figure 4-1. Clock Mode Operation

Clock Mode Sel 1	Clock Mode Sel 0	Clock Mode	Operation
0	0	0	Internal Clock not driving P2
0	1	1	External Clock
1	0	2	Not recommended
1	1	3	Internal Clock driving P2

Typically, Clock Mode 0 is used for single-axis applications, since it uses the internal clock source and does not drive the 10 MHz Clock In/Out pin on the P2 connector.

Async Mode

The AOH/OCLK line on the 10897B board can be programmed

- to be off (an input that does nothing),
- to operate as an asynchronous hold input, or
- as a position output clock. Refer to Figure 4-2, Async Mode Operation.

Async Mode 0 causes the AOH/OCLK to be an input that does nothing. This is the off mode.

As an asynchronous hold input (Async Mode 1), the P2 position output lines will be guaranteed stable and holding within 120 ns of AOH/OCLK going high. In this mode the 10897B board will drive the Output Hold line which may be tied to the Output Hold lines of other "slave" 10897B boards, allowing simultaneous synchronous sampling of multiple axes by an asynchronous input.

NOTE

Sampling here actually means "holding" of the P2 36-bit position outputs and does not cause sampling of the internal 35-bit position registers. For this situation, the "slave" 10897B boards must be in Async Mode 0, 2, or 3 and bit 7 of the Output Hold and Rate Control Register must be set to 1.

In the position output clock modes (Async Modes 2 and 3), the AOH/OCLK line may be used to clock position data into the user's register. In Async Mode 2, the AOH/OCLK line follows the Output

Hold waveform after a 1 clock cycle (100 ns) delay. Async Mode 2 is suitable only when the Output Hold and Rate Control register is set for a position output rate of less than 10 MHz. To clock position data into the user's register at 10 MHz, Async Mode 3 is used.

Async Mode Sel 1	Async Mode Sel 0	Async Mode	Operation
0	0	0	Off
0	1	1	Asynchronous Hold Input
1	0	2	Output Clock - less than 10 MHz Output Rate
1	1	3	Output Clock at 10 MHz Output Rate

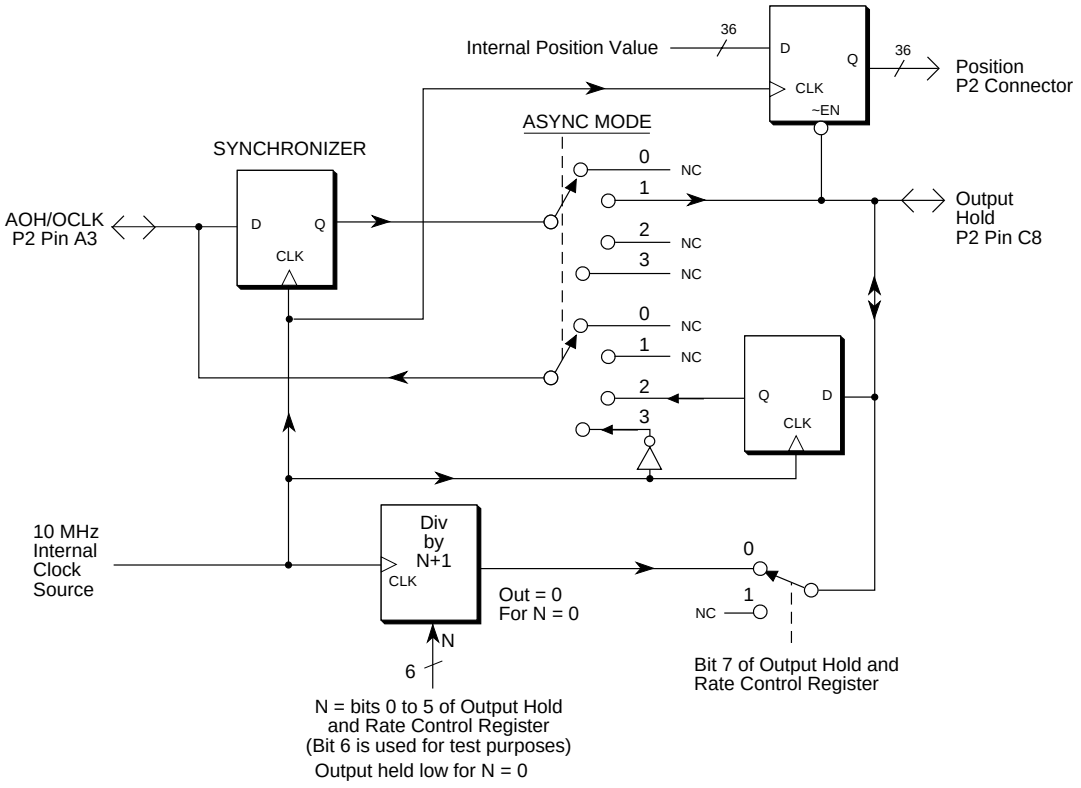


Figure 4-2. Async Mode Operation

Window Mode

The output modes for the Window output line are described as shown below.

Window Mode Sel 2	Window Mode Sel 1	Window Mode Sel 0	Window Mode	Output Format
0	0	0	0	Open Collector High True
0	0	1	1	TTL Low True
0	1	0	2	TTL High True
0	1	1	3	3-State
1	0	0	4	Open Collector High True Latched
1	0	1	5	TTL Low True Latched
1	1	0	6	TTL High True Latched
1	1	1	7	3-State Latched

NOTE For Window and Error Mode, Latched = Held by Output Hold.

Error Mode

The output modes for the P2 Error output line are shown below. Refer to the P2 Error Mask Register section for more information.

Error Mode Sel 2	Error Mode Sel 1	Error Mode Sel 0	Error Mode	Output Format
0	0	0	0	Open Collector Low True
0	0	1	1	TTL Low True
0	1	0	2	TTL High True
0	1	1	3	3-State
1	0	0	4	Open Collector Low True Latched
1	0	1	5	TTL Low True Latched
1	1	0	6	TTL High True Latched
1	1	1	7	3-State Latched

~Bus Mode

The ~Bus Mode bit determines how the position output bits and any other output bits programmed in 3-state mode are enabled.

When ~Bus Mode is low, 3-state and position outputs are enabled when ~Read is low and the P2 address inputs match the value written into the P2A0-3. This is used when multiple 10897B boards are present in a backplane and the outer rows of the P2 connector are bussed together. Each 10897B board (up to a maximum of 16) can have its own address; therefore, its P0–P35 outputs may be read separately over a common bus.

When ~Bus Mode is high, the 3-state and position outputs are enabled when ~Read is low. In this mode the P2 address inputs are not used and the P0–P35 pins on the P2 connector may not be bussed together when multiple 10897B boards are present in the one backplane.

P2 A0-3

These bits comprise the address to which the hardware position and 3-state outputs will respond when in Bus Mode.

Command Register

The Command Register is a write-only register. Bits that are set in the value written to the Command Register will cause the actions defined as shown below.

Bit	15	14	13	12	11	10	9	8
Function	not used	not used	not used	not used	not used	not used	not used	Reset Position

Bit	7	6	5	4	3	2	1	0
Function	Sample Velocity 2	Sample Velocity 1	Sample Position 6	Sample Position 5	Sample Position 4	Sample Position 3	Sample Position 2	Sample Position 1

Any combination of commands may be executed with a single write to the command register. Writing a value of zero does nothing.

Interrupt Vector Register

The Interrupt Vector register is loaded with the value to be asserted on the data bus during an interrupt acknowledge cycle. This register may also be read by a data transfer cycle. Note that since it is an eight-bit register and data transfer cycles are D16 or D32 cycles, the upper bits of data will be invalid during a data read cycle.

Position Offset Register

This register is used in two ways:

- to preset the value in the position counter (see Preset Enable in the General Control/Status Register section), or
- to offset (subtract from) the position counter value to create the 36-bit hardware position outputs P0–P35

MSB Position Offset Register

This register holds the three MSBs for the position offset value when the Position Offset LSBs Register is used to load the position offset value (see Sign Extend Position Offset Register below for the other way to load the position offset value). Only the three LSBs of this register are significant. The actual loading of the position offset register occurs during the write to the LSBs register, therefore the MSB Position Offset register must be written to first. During a read of this register, the MSBs of the actual offset register are read, not the holding value. The Position Offset MSBs Register may be written to or read using a D32 data transfer at address $80 or a D16 data transfer at address $82.

LSB Position Offset Register

A write to this register will cause the value written to be concatenated with the Position Offset MSBs register and the resultant 35-bit value to be loaded into the Position Offset register. This register may be written to or read using the D32 or two D16 data transfers. When using D16 data transfers to write to this register, the write to the LSBs, D 0-15, causes the actual register update. The MSBs, D16-31, must therefore be written first.

Sign Extend Position Offset Register

A write to this register will cause the value written to be sign-extended to 35 bits and the resultant value to be loaded into the Position Offset register. This register may be written or read using a D32 or two D16 data transfers. Note that when using D16 data transfers to write this register, the write to the LSBs, D0-15, causes the actual register update. The MSBs, D16-31, must therefore be written first.

Clip and Window Mask Register

The Clip and Window Mask Register is a 32-bit register that contains the bits for the Clip and Window Masks. Though the Clip Mask occupies bits 0 through 15 and the Window Mask bits 16 through 30, the entire register must be written as a whole using one D32 data transfer or two D16 data transfers with the MSBs sent first.

Clip Mask

The 10897B board can limit its hardware position output LSBs to a saturation limit value when the actual output value exceeds the value that can be expressed by those bits. When this option is programmed, the selected low order bits function normally until their range is exceeded, at which point they retain their maximum value (high order bits are unaffected). Figure 4-3, Position Output Clipping, shows this.

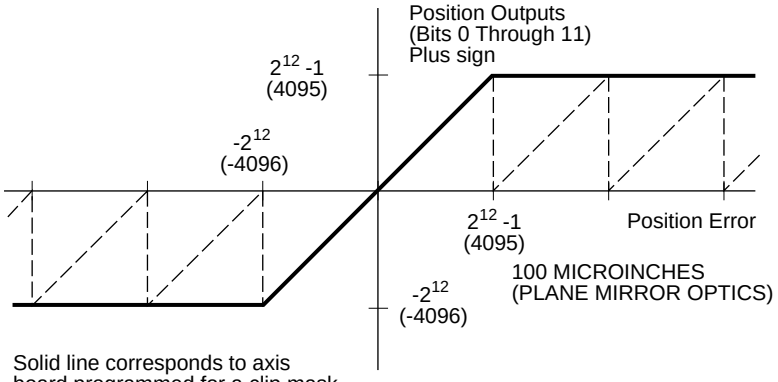


Figure 4-3. Position Output Clipping

This feature is controlled by the Clip Mask bits. The following table defines the valid clip mask values and the usage of output bits for each value.

Clip Mask Value	Output Usage
$FFFF	No Clipping - Use All Bits
$FFFE	Use MSB and 8 LSBs
$FFFC	Use MSB and 9 LSBs
$FFF8	Use MSB and 10 LSBs
$FFF0	Use MSB and 11 LSBs
$FFE0	Use MSB and 12 LSBs
$FFC0	Use MSB and 13 LSBs
$FF80	Use MSB and 14 LSBs
$FF00	Use MSB and 15 LSBs
$FE00	Use MSB and 16 LSBs
$FC00	Use MSB and 17 LSBs
$F800	Use MSB and 18 LSBs
$F000	Use MSB and 19 LSBs
$E000	Use MSB and 20 LSBs
$C000	Use MSB and 21 LSBs
$8000	Use MSB and 22 LSBs
$0000	Use MSB and 23 LSBs

Window Mask

The 10897B board can generate a Window output signal. This signal is true whenever the hardware position output value is within range of the value specified by the Window Mask. The Window Mask and associated range values are defined as shown below.

Window Mask Value	Signed Magnitude Range	Two's Complement Range
$7FFF	mag(P) < 1	-2 < P < 1
$7FFE	mag(P) < 2	-3 < P < 2
$7FFC	mag(P) < 4	-5 < P < 4
$7FF8	mag(P) < 8	-9 < P < 8
$7FF0	mag(P) < 16	-17 < P < 16
$7FE0	mag(P) < 32	-33 < P < 32
$7FC0	mag(P) < 64	-65 < P < 64
$7F80	mag(P) < 128	-129 < P < 128
$7F00	mag(P) < 256	-257 < P < 256
$7E00	mag(P) < 512	-513 < P < 512
$7C00	mag(P) < 1024	-1025 < P < 1024
$7800	mag(P) < 2048	-2049 < P < 2048
$7000	mag(P) < 4096	-4097 < P < 4096
$6000	mag(P) < 8192	-8193 < P < 8192
$4000	mag(P) < 16384	-16385 < P < 16384
$0000	mag(P) < 32768	-32769 < P < 32768

Test Rate A and B Registers

The Test Rate A and B registers control the frequency of the Test Rate A and Test Rate B signals, which are selectable as Measurement A and Measurement B inputs to the resolution extension circuitry. Bit 9 of these registers are enable bits and bits 0 through 8 determine the frequency. The frequency will be 40 MHz/(N+1). where N is the binary value in bits 0 through 8.

Sample Delay Register

The 10897B board contains six position registers and two velocity registers that are read over the VMEbus and may be sampled by hardware or software. The Sample Delay Register determines the amount of delay in the sample path for each register. A one in any bit position of the Sample Delay Register corresponds to a 100 ns delay while a zero increases the delay to 600 ns, which helps match the delay in the sample path to the delay in the data path. The bit positions and the registers they control are defined as shown below.

Bit	7	6	5	4	3	2	1	0
Register	Vel 2	Vel 1	Pos 6	Pos 5	Pos 4	Pos 3	Pos 2	Pos 1

Note that when using the Auto-Sample feature (described in the Position and Velocity Registers section), the delay bit for the register being Auto-Sampled must be set to Minimal (one).

Sample Mode and Mask Register

The bits in the Sample Mode and Mask register are defined as shown below.

Bit	15	14	13	12	11	10	9	8
Function	Vel 2 Sample Mode	Vel 1 Sample Mode	Pos 6 Sample Mode	Pos 5 Sample Mode	Pos 4 Sample Mode	Pos 3 Sample Mode	Pos 2 Sample Mode	Pos 1 Sample Mode

Bit	7	6	5	4	3	2	1	0
Function	Vel 2 IRQ Enable	Vel 1 IRQ Enable	Pos 6 IRQ Enable	Pos 5 IRQ Enable	Pos 4 IRQ Enable	Pos 3 IRQ Enable	Pos 2 IRQ Enable	Pos 1 IRQ Enable

Sample Mode bits

When a position or velocity register is sampled—by asserting ~sample on the P2 hardware connector or by writing to the VME command register, its bit associated in the Sample Status register will go high. When the VME position or velocity register is read, its associated bit will go low.

The Sample Mode bits define the sample mode for each of the six position and two velocity registers. When a register's sample mode bit is zero, that register will be updated any time a hardware or software sample takes place for that register. When a register's sample mode bit is one, that register will be updated only when its associated bit in the Sample Status Register is low (that is, the prior sample has been read).

Sample Mask bits

The Sample Mask bits determine which registers will generate an IRQ while their associated bits in the Sample Status Register are high.

Sample Status Register

When a position or velocity register is sampled, the bit associated with that register in the Sample Status register will go high. When the register is read, its associated bit will go low. The bits in the Sample Status Register and their association with the position and velocity registers are defined as shown below.

Bit	7	6	5	4	3	2	1	0
Register	Vel 2	Vel 1	Pos 6	Pos 5	Pos 4	Pos 3	Pos 2	Pos 1

IRQ Error Mask Register

The IRQ Error Mask Register determines which error indicators will cause an interrupt request. The bits in the IRQ Error Mask Register are defined in the table below.

Bit	7	6	5	4	3	2	1	0
Register	not used	INTRP UNLOCK	OVFL	GLITCH	-Vb	+Vb	-Va	+Va

The error indicators are discussed in the Error Status and Reset Register section.

P2 Error Mask Register

The P2 Error Mask Register determines which error indicators will cause the P2 Error line to go active. The bits in the P2 Error Mask Register are defined as shown below.

Bit	7	6	5	4	3	2	1	0
Function	not used	INTRP UNLOCK	OVFL	GLITCH	-Vb	+Vb	-Va	+Va

Error Status and Reset Register

The Error Status and Reset Register is a read-write register through which you can read or reset the 10897B board's error indicators. If an error occurs causing an Error Indicator bit to go true, that bit remains true until it is reset.

Bits 0 through 5 (+Va, -Va, +Vb, -Vb, GLITCH, and OVFL) are reset by writing to the Error Status and Reset Register (the value written containing bits set corresponding to the indicator you want to reset). The bits in the Error Status and Reset Register are defined as shown below.

Bit	7	6	5	4	3	2	1	0
Function	INTRP RESET	INTRP UNLOCK	OVFL	GLITCH	-Vb	+Vb	-Va	+Va

+Va and +Vb

The +Va and +Vb bits indicate that the Measurement A or Measurement B input circuitry has detected two positive transitions that were less than 26.7 ns apart and thus the measurement may be invalid.

-Va and -Vb

The -Va and -Vb indicate that the Measurement A or Measurement B input circuitry has not detected a transition in 12.8 µs and thus the measurement may be invalid. When either of these conditions is true, the corresponding signal loss LED will illuminate on the front panel. Similarly, when these bits are cleared, the LEDs will turn off.

Glitch

The GLITCH bit indicates that an excessive acceleration has occurred (probably due to a measurement signal glitch) and thus the measurement may be invalid.

OVFL

The OVFL bit indicates the position counter has overflowed.

INTRP UNLOCK

The INTRP UNLOCK bit indicates the interpolation circuitry has lost lock and thus the measurement may be invalid.

INTRP RESET

The INTRP RESET bit indicates the state of the interpolator reset line. This line is controlled by bit 6 of the value written to the Error Status and Reset register. The INTRP UNLOCK bit is reset only by an interpolator reset. This is done by writing a value to the Error Status and Reset Register with bit 6 set and then another one with bit 6 cleared.

Output Hold and Rate Control Register

The 10897B board generates position at at 10 MHz rate. This rate may be reduced by using the Output Hold line. In addition, the 10897B board can be programmed to drive the Output Hold line such that when it is asserted for N 100-ns cycles and then negated for one cycle, where N is a number from 0 to 63.

Bit 7 of the Output Hold and Rate Control register determines whether or not the output rate generator will drive the Output Hold line. If bit 7 is set to a one, the output rate generator will not drive the Output Hold line and the user may or may not be allowed to drive it, depending on the setting of Async Mode in the Output Control register.

If bit seven is set to zero, the line will be driven by the 10897B board and the user must not attempt to drive it. Note that when Bit 7 of the Output Hold and Rate Control register is set to a zero, the Async Mode in Output Control register must not be set to Mode 1. Refer to Async Mode in the Output Control Register section.

To cause the 10897B board to drive the Output Hold line at a rate of 10/(N+1) MHz, the Output Hold and Rate Control register is simply loaded with the value N (N being 63 or less).

To use the Output Hold line as an input and therefore to control it externally, the Output Hold and Rate Control register should be loaded with 128 (that is, bit 7 = 1, all other bits = 0).

A Reset of the 10897B board will initialize this register to 128.

Filter Control Register

The 10897B board can filter the position data it generates. This may be useful when a laser system employs many axes and the laser measurement signal contains more noise due to the lower intensity of the light entering the laser measurement receiver. The 10897B board's filter is implemented such that the delay through the filter is zero at constant velocities. Offsets introduced by the filter occur only during acceleration and are relatively small.

The filter is controlled by the Filter Control register. The bits in the Filter Control register are defined as shown below.

Bit	7	6	5	4	3	2	1	0
Function	not used	not used	not used	Filter Init	Kp1	Kp0	Kv	Filter On

Filter On

The Filter On bit enables the filter when set to one. When the Filter On bit is set to zero, the filter is taken out of the data path but is still used to detect measurement signal glitches. The filter constants will therefore always determine the acceleration threshold that will cause a GLITCH error indication.

Kv and Kp

The Kv bit specifies the velocity feedback constant for the filter and the Kp bits specify the position feedback constant. The effects of different filter constants on glitch threshold, following error, relative filtering, and relative damping are shown below.

Filter Init

The Filter Init bit is used to initialize the filter. Any time a measurement glitch occurs, the filter must be initialized. This is done by writing a 1 to the Filter Init bit after the measurement signals have been restored.

Note that the Filter Init bit is write only and will always read zero.

					Glitch Threshold					
Kp1	**Kp0**	**Kv**	**Kp Value**	**Kv Value**	**Linear Optics**	**Plane Mirror Optics**	**High Res. Optics**	**Following Error**	**Filtering Score**	**Damping Score**
0	0	0	2-7	2-14	100 g	50 g	25 g	1.6 nm/g	8	2
0	1	0	2-6	2-14	100 g	50 g	25 g	1.6 nm/g	6	4
1	0	0	2-5	2-14	100 g	50 g	25 g	1.6 nm/g	4	6
1	1	0	2-4	2-14	100 g	50 g	25 g	1.6 nm/g	2	8
0	0	1	2-7	2-13	200 g	100 g	50 g	0.8 nm/g	7	1
0	1	1	2-6	2-13	200 g	100 g	50 g	0.8 nm/g	5	3
1	0	1	2-5	2-13	200 g	100 g	50 g	0.8 nm/g	3	5
1	1	1	2-4	2-13	200 g	100 g	50 g	0.8 nm/g	1	7

For more complete information on the filter, contact Agilent.

Overflow Level and Output Format Register

The bits in the Overflow Level and Output Format Register are defined as shown below.

Bit	7	6	5	4	3	2	1	0
Function	not used	not used	not used	not used	not used	Output Format	OVFL Level 1	OVFL Level 0

Overflow Level

The 10897B board is capable of generating overflow errors for any one of four ranges. These ranges are defined as shown below.

OVFL Level 1	OVFL Level 0	Valid Bits	Valid Range
0	0	32	-2^{31} thru $2^{31}-1$
0	1	33	-2^{32} thru $2^{32}-1$
1	0	34	-2^{33} thru $2^{33}-1$
1	1	35	-2^{34} thru $2^{34}-1$

NOTE

The ranges specified are for the position counter and position registers. If the offset register contains a non-zero value then the hardware position output value will need one more bit to represent all valid position output values.

Output Format

The 10897B board's hardware position output bits can be programmed to operate in 2's-complement or signed-magnitude format. This is determined by the Output Format bit in the Overflow Level and Output Format Register. A zero in this bit will select 2's-complement while a one will select signed-magnitude. In signed-magnitude format, P35 is the sign bit and is high when the output value is negative.

Position and Velocity Registers

The 10897B board contains six position and two velocity registers that may be read over the VME backplane. The base addresses for these registers are defined as shown below.

Address	Register
$100	Position 1
$104	Position 2
$108	Position 3
$10C	Position 4
$110	Position 5
$114	Position 6
$118	Velocity 1
$11C	Velocity 2

Each of these registers may be Auto-Sampled during a read operation. This function is controlled by bit five of the address bus. To enable the Auto-Sample feature, add $20 to the base address of the register being read. When the position or velocity registers are read with Auto-Sampling using 16-bit transfers, the sample operation occurs during the read of the MSBs.

Note that when using the Auto-Sample feature, the delay bit in the Sample Delay Register for the register being read must be set to one.

The 10897B board's position registers are 35 bits wide. During read operations these registers may be aligned to the 32-bit VME data bus with one of four possible alignments. The alignment is controlled by address bits 6 and 7. When a register is read at its base address, the 32 LSBs of the register are read. For each incremental addition of $40 to the base address of the register being read, an LSB is dropped and an MSB is added. This is shown below.

Address Offset	Position Bits Read
$00	31:0
$40	32:1
$80	33:2
$C0	34:3

The 10897B board's velocity registers contain 25 bits of velocity data. Bits 0 to 24 contain the velocity data and bits 25 to 31 are sign-extended from bit 24. Since the velocity data is only 25 bits wide, there is no need to shift the alignment of the velocity bits when reading like there is when reading the 35-bit position registers. The units of velocity are based on the difference in position over a 100 ns period and may be determined by multiplying the value from the velocity register by

$$\lambda/(F \times 2^{22} \times 100 \text{ ns})$$

where λ = laser wavelength $\cong$ 632.991 nm

F = Fold factor, based on the optics used

- F = 2 for linear optics
- F = 4 for plane mirror optics
- F = 8 for high resolution plane mirror optics

5

Theory of Operation

Introduction

This chapter provides limited information about how the Agilent 10897B High Resolution VMEbus Laser Axis Board functions. This theory of operation assumes some familiarity with both laser measurements and VMEbus operation and terminology, explaining only how this board works. Refer to the VMEbus Specification for descriptions of the VMEbus specifications and terms. Refer to the Agilent Laser and Optics Users Manual for explanations of laser measurements and optics operation.

NOTE

The information contained in this chapter is provided to help in the interface-design process. It can also be used to troubleshoot hardware and software problems that are related to the design process.

Simplified Block Diagram

Figure 5-1 shows the functional block diagram for the Agilent 10897B High Resolution VMEbus Laser Axis Board. The main components of the Board are the VMEbus Interface, Laser Axis Processing Unit, and Front-Panel Input/Output. These blocks are described in the following paragraphs.

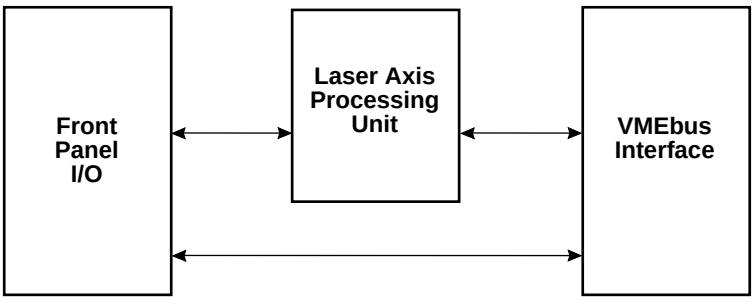


Figure 5-1. Agilent 10897B Simplified Block Diagram

VMEbus Interface

The VMEbus Interface links the Agilent 10897B board's laser axis function to the VMEbus structure. It handles all interactions between the 10897B board and the VMEbus master. The 10897B board appears as a slave to the VMEbus master.

The VMEbus Interface hardware block contains six functional sections. The main one is the Location Monitor and Decode section, which monitors bus activity and responds to appropriate bus cycles. Connected to the location monitor are the Base Address Switches (S1 and S2).

The Interrupt Request Logic monitors the laser system status and generates VMEbus interrupt requests when specified errors occur.

The Interrupt Vector Register is used during interrupt acknowledge cycles to indicate which routine will process laser system errors.

The Data Transceivers simply connect the board's local 32-bit data bus to the 32-bit VME data bus.

Finally, the Lo to Hi Bit Transceivers interconnect the upper 16 and lower 16 bits of the local data bus allowing operation with a 16-bit VME data bus.

Agilent Laser-Axis Processing Unit

The Agilent Laser Axis Processing Unit generates real-time position information from the laser input signals and stores this data in the appropriate holding registers for retrieval. It also tests the integrity of measurement input data.

Front-Panel Input/Output

The Front-Panel Input/Output receives measurement input signals and isolates these inputs from the internal Agilent 10897B board's circuitry. Additionally, this block determines if the Meas 1 and Meas 2/Ref input signals are present and drives or receives the four-line Common Laser Signals and Receiver Power Distribution provided by the 16-pin ribbon connector.

6

Maintenance

Introduction

This chapter provides maintenance information for the Agilent 10897B High Resolution VMEbus Laser Axis Board.

Maintenance

No maintenance is required.

Calibration

The Agilent 10897B board requires no periodic calibration.

Troubleshooting

Refer to the Trouble Isolation procedure in Chapter 9 of this manual to diagnose and repair the Agilent 10897B board.

7

Replaceable Parts

Introduction

This chapter provides a listing of assembly-level replaceable parts for the Agilent 10897B High Resolution VMEbus Laser Axis Board and information on how to order replaceable parts.

Ordering Information

To obtain replaceable parts, address your order to your nearest Agilent Technologies Sales or Service office. Identify parts by Agilent part number.

Agilent 10897B Exchange/Rebuilt Assembly

Agilent Technologies has an exchange/rebuilt Agilent 10897B available, Agilent Part Number 10897-69002. (This exchange/rebuilt assembly consists of all the assembly replaceable parts except interconnect cables and manual.)

Agilent 10897B Options

All options for the Agilent 10897B have Agilent Part Numbers. The following part numbers can be used to order replacement axis-interconnect cables for options 002 through 007 and the English or Japanese Agilent 10897B Operating and Service manuals.

Table 7-1. Agilent 10897B Option Part Numbers

Part Number	Option	Description
10895-60201	002	2-Axis Interconnect Cable
10895-60202	003	3-Axis Interconnect Cable
10895-60203	004	4-Axis Interconnect Cable
10895-60204	005	5-Axis Interconnect Cable
10895-60205	006	6-Axis Interconnect Cable
10895-60210	007	7-Axis Interconnect Cable
10897-90010	AV4	English Operating and Service manual
10897-90011	ABZ	Japanese Operating and Service manual

8

Manual Changes

Introduction

This chapter provides information necessary to update the manual for newer products and to backdate the manual for older products.

Manual Changes

This manual applies directly to units having serial number prefix 3332. For units with a different serial number prefix, refer to the following paragraphs.

Newer Products

New products may have higher serial number prefixes than that listed on the title page of this manual. The manuals shipped with these units will include a "Manual Changes" sheet that describes all required manual changes. If the updating information is missing, contact the nearest Agilent Technologies Sales and Service office for information.

Older Products

As of the date of this manual, there are no older versions of the Agilent 10897B product.

9

Service

Introduction

Use the information in this chapter along with the information provided in Chapter 5 for interface-design problem solving and related maintenance.

Trouble Isolation

If the Agilent 10897B High Resolution VMEbus Laser Axis Board is known to be defective, you can:

- return it to an Agilent Service Center for repair, or
- exchange it by ordering 10897B exchange part number 10897-69002.

Use the following procedure for troubleshooting:

1 Ensure that correct board addressing is being executed (program the user LED to verify correct addressing).

2 Ensure that the Meas 1 and Meas 2 signal LEDs (green) are lit, indicating that signals are present.

3 Ensure that +5 Vdc (+0.25 V, -0.125 V) is present on the VMEbus backplane.

The Laser and Optics Users Manual should be used to properly configure the system laser head and optics. A complete set of laser optics specifications and limitations are included in the Laser and Optics Users Manual.

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Service and Support

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Technical information for test and measurement products and services is available 24 hours a day, 7 days a week, by calling **1-800-800-5281.**

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Printed in U.S.A
Data subject to change
Rev 12/99

DECLARATION OF CONFORMITY

According to ISO/IEC Guide 22 and CEN/CENELEC EN 45014

Manufacturer□s Name: Agilent Technologies, Inc.

Manufacturer□s Address: Santa Clara Site
5301 Stevens Creek Boulevard
Santa Clara, California 95052-8059
U.S.A.

Declares, that the product

Product Name: VMEbus Laser Positioning System, consisting of:

Model Number: 10895A Axis Board, 10896B Compensation Board, 10897B Axis Board, 10780C/F Remote Receiver, 10751A/B/C/D Air Sensor, 10757A/B/C/D/E/F Material Sensor, 10884A Power Supply

Product Options: This declaration includes all product options.

Conforms with the following product specifications:

EMC	Standard	Limit
	CISPR 22: 1997 / EN 55022:1994 +A1, A2	Class A
	IEC 1000-4-2:1995 / EN 50082-1:1997	4kV CD, 8kV AD
	IEC 1000-4-3:1995 / EN 50082-1:1997	3 V/m, 1kHz 80% AM, 26-1000 MHz
	IEC 1000-4-4:1995 / EN 50082-1:1997	0.5kV signal lines, 1kV power lines
	EN 61000-3-2: 1995	Class A
	EN 61000-3-3: 1995	
Safety	IEC 1010-1: 1990 + A1 / EN 61010-1: 1993	
	IEC 825-1:1993 +A1 / EN60825-1:1994 +A11, Class 2	

Supplementary Information:

The product models listed above comply with the requirements of the Low Voltage Directive 73/23/EEC, the EMC Directive 89/336/EEC and carry the CE marking accordingly.

December 19, 1995
Date

Bruce Euler
Bruce Euler, Quality Engineering Manager

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Continued from front matter. . .

Warranty (contd)

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Safety Considerations (contd)

WARNING

INSTRUCTIONS FOR ADJUSTMENTS WHILE COVERS ARE REMOVED AND FOR SERVICING ARE FOR USE BY SERVICE-TRAINED PERSONNEL ONLY. TO AVOID DANGEROUS ELECTRIC SHOCK, DO NOT PERFORM SUCH ADJUSTMENTS OR SERVICING UNLESS QUALIFIED TO DO SO.

Acoustic Noise Emissions

LpA<47 dB at operator position, at normal operation, tested per EN 27779. All data are the results from type test.

Geräuschemission

LpA<47 dB am Arbeits platz, normaler Betrieb, geprüft nach EN 27779. Die Angagen beruhen auf Ergebnissen von Typenprüfungen.

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Manual Part Number 10897-90010

Printed in U.S.A, AUGUST 2000